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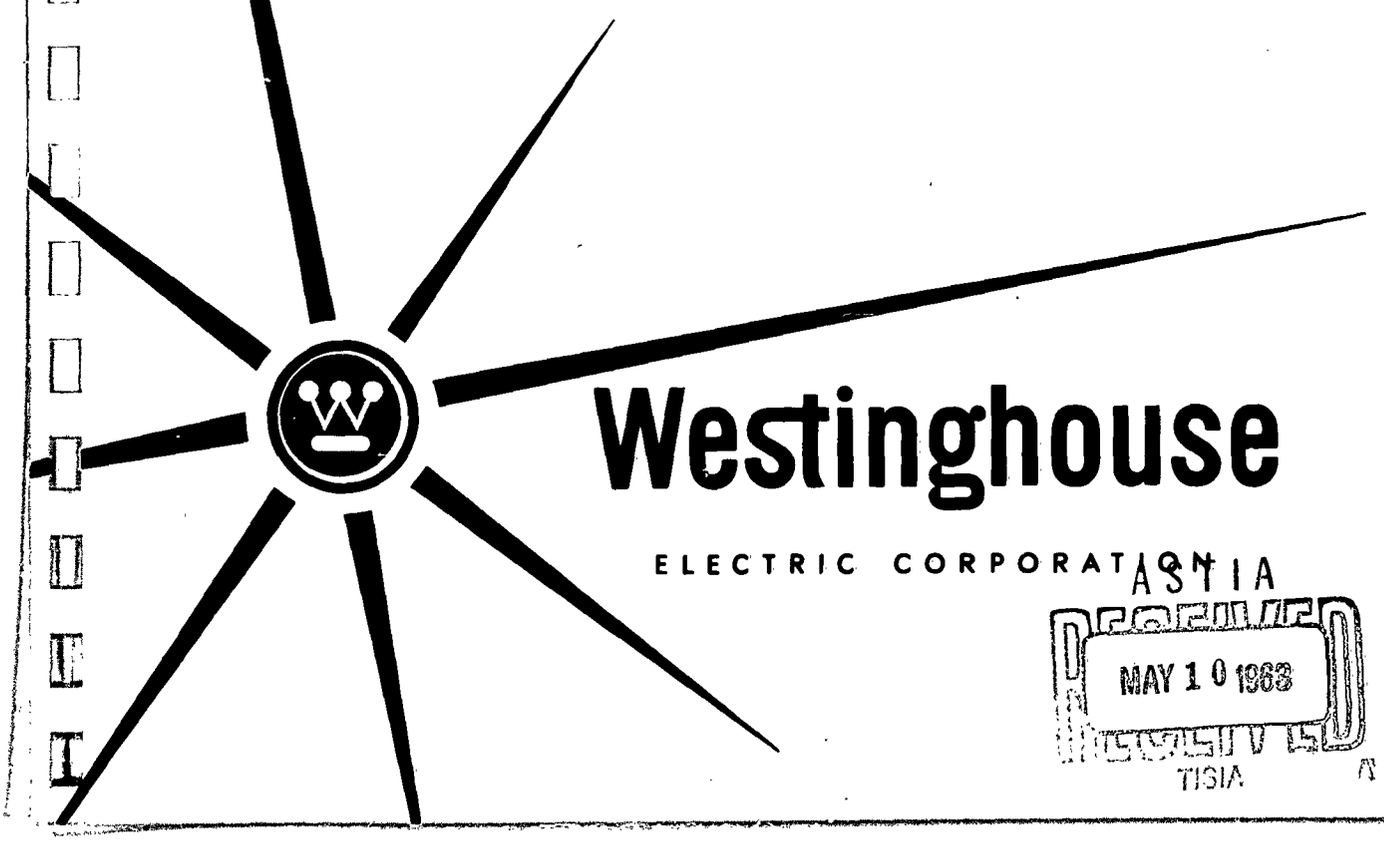

Westinghouse

ELECTRIC CORPORATION

THIRD INTERIM DEVELOPMENT REPORT
FOR
STUDY OF FABRICATION
OF MICROELECTRIC ASSEMBLIES
FOR FREQUENCY AND TIME CONTROL
SYSTEMS

This report covers the period 1 Jan 1963 to 29 March 1963

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WESTINGHOUSE ELECTRIC CORPORATION
ELECTRONICS DIVISION

P. O. Box 1897

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ABSTRACT

The purpose of this program is to design a family of microelectronic blocks for time and frequency control equipment. Various microelectronic fabrication techniques of packaging are presented. Specifications for digital and analog circuits are given. Interim results of a crystal filter evaluation are presented.

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1. PURPOSE

The purpose of this program is to design microelectronic building blocks that can be used to construct closely related equipments used in time and frequency control. The equipments are specified in SHIPS-A-4104. The interlocking factors of cost, performance, availability, fault location, and repair procedure of the various microelectronic approaches are to be evaluated. The work is to culminate in designs for the required circuits and recommendation of a specific microelectronic approach.

2. GENERAL FACTUAL DATA

2.1 IDENTIFICATION OF PERSONNEL

The following persons have contributed to the program during the report period:

Name	Title	Man Hours
G. Reed Brainerd	Section Manager	33.0
Robert M. Frazier	Senior Engineer	4.0
Wayne R. Olson	Senior Engineer	216.0
Renato V. Salcedo	Engineer	398.0
Edward H. Hooper	Engineer	13.0
William W. Young	Engineer	6.0
George A. Sporzynski	Associate Engineer	408.0
Kenneth Peterson	Associate Engineer	306.0
Larry Koenig	Associate Engineer	63.0
Robert J. Taylor	Assistant Engineer	383.0
Earl Heitman	Technician	17.0
Edwin Melvin	Technician	20.0

2.2 REFERENCES

(1) Designing Unneutralized Tuned Transistor Amplifiers by Use of a Westinghouse Developed Test Set, R. M. Frazier, Westinghouse Electronics Division - Report No. 306.6, March 1958.

(2) Handbook of Semiconductor Electronics, Lloyd P. Hunter, McGraw-Hill Book Co., 1956, P. 11-22.

(3) Radio Engineers Handbook, Frederick E. Terman, McGraw-Hill Book Co., 1943.

3.1 DETAILED FACTUAL DATA

3.1 CIRCUIT LOADING REQUIREMENTS

All systems have been studied and a table defining the loading requirements for all circuits has been assembled. The table appears in Appendix A.

3.2 MICROELECTRONIC PACKAGING STUDY

3.2.1 General Considerations

The problem of making satisfactory electrical connections presents a very serious challenge to the designer of microminiature systems. As the size of circuits decreases, the number of interconnecting wires remains relatively fixed. The bulk of these wires and the connectors associated with them place a practical limit on the size of these systems.

One obvious solution to this problem is to reduce the size of the wires and connectors. However, a level is soon reached when the wires and connectors becomes so small that conventional handling techniques cannot be used. Furthermore, small diameter wires break easily and can handle only a limited amount of current. Therefore, other methods of interconnections must be investigated.

When seeking a new connection scheme, it is important to keep in mind the basic objectives of microminiature circuits. Connections are just as important as circuit elements. A bad connection will cause circuit failure as readily as a bad component. Hence, as much care should be put into the design of connectors as into circuit design.

An interconnection scheme has been developed with the following objectives in mind:

(1) The highest possible reliability consistant with the other requirements.

(2) The maximum possible packaging density with reasonable power dissipation per unit volume.

(3) Easy fabrication and repair of the system.

(4) Ease of layout of the conventional circuit in the interconnection scheme.

(5) Low material and assembly costs.

To achieve these goals, the packaging approach is organized on two separate levels. On the first level, the individual circuit wafers are soldered into modules. On the second level, the modules are interconnected to form the system. Modules are connected by means of plugs, hence, they are easily removable from the system. When a malfunction occurs, the module at fault is simply replaced with a new one. This keeps down time very low. The

circuit wafers which make up each module are interconnected on a more permanent basis. Eventually, modules will be throw-away. For the present, the modules will be repaired after they have been removed from the system.

The interconnection system described has been kept as general as possible to accommodate any of the large number of miniaturization approaches. Any flat package configuration can be used. Figure 1 shows the dimensions of a typical substrate. In addition, discrete components, such as inductors, which cannot be fabricated by microminiature techniques can also be packaged. Small crystal filters are also compatible with this approach.

Section 3. 2. 2 explains in detail the assembly of circuit wafers into modules. Section 3. 2. 3 deals with an interconnection scheme for the modules.

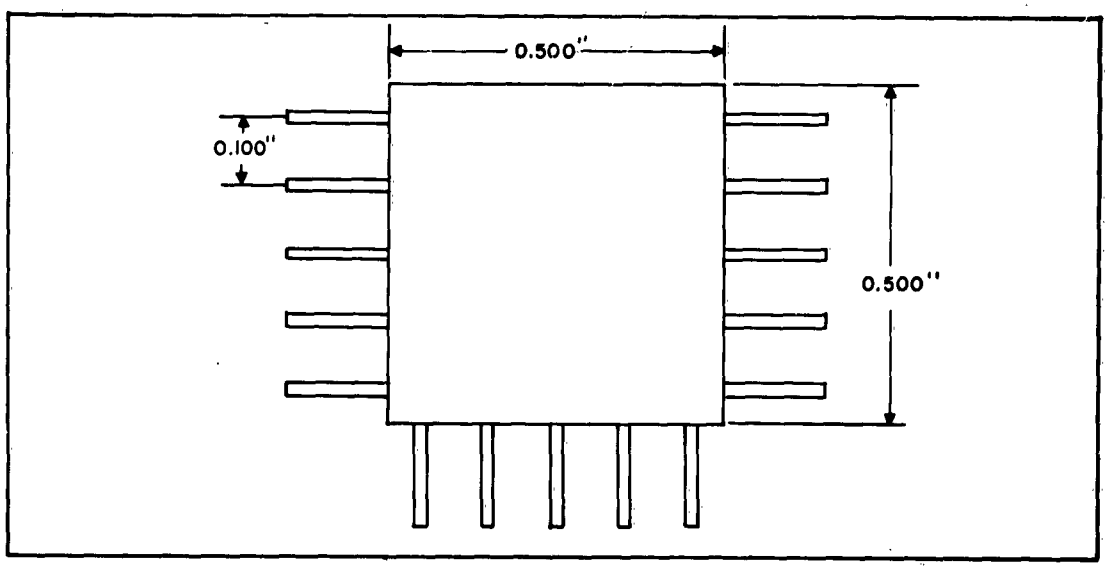

Figure 1. Dimensions of Flat Package

3. 2. 2 Interconnection of Wafers

The first level of interconnections, the assembly of wafers into modules, is examined in this section. A typical module consists of a number of circuit substrates, filters, and inductors connected in a semi-permanent fashion. The size of such a module is a function of many factors. On the one hand are such economic considerations as: cost of individual wafers, reliability of wafers, skill of maintenance personnel, and cost of storing spares. On the other hand, system factors such as length of leads, coupling between adjacent circuits, heat dissipation, and logical breakdown of the system into functional units, will determine the size of a module.

In general, the system is first broken down into functional groups or areas and these are assembled into modules. The procedure for an analog system will differ from that for a digital system. In an analog system, modules are generally designed around components such as filters or other non-standard items. Digital systems in general do not have such components. Instead, a group of circuits which is repeated very often is used as a module.

Basically, there are two types of connections available: welded or soldered connections. Variations of these yield several systems which are discussed next.

Welded Joints - the most straightforward approach is point-to-point wiring and welded joints. The wafers are stacked up such that all leads are aligned. Short lengths of wire are welded to the leads to form the required connections. This scheme requires relatively little volume for connections and the materials used (wires) are very cheap. Furthermore, welded joints are very reliable. Offsetting these desirable characteristics are some serious disadvantages. Welding small joints is a very precise operation requiring special machinery and skilled personnel. Presently, all joints are welded by hand which makes the entire operation very expensive.

Short wires are self supporting; however, long wires would need additional support. Repair of the modules is possible; however, much cutting and welding is needed to replace a substrate in a module. Since all operations are made by hand, wiring mistakes during assembly and repair can easily be made.

Deposited Connections Approach - The wafers are arranged as in the previous case. Next, the leads are cut flush with the edges of the wafers. The three sides of the wafer stack which contain the leads are ground down to a fine optical finish. The interconnection pattern is then deposited by thin film techniques. A variation of this method is to plate the stack with copper and then selectively etch the copper away by standard printed circuit techniques or by means of an electron beam. The results of all three processes are similar. Since only one layer of wiring is allowed, interconnections are limited. Repair of the module is possible only if the module is reground and replated after the faulty substrate is replaced. Although systems such as this have been built, a question remains whether the connections made in this manner are reliable. The area of contact is only as large as the area of the wires. Any slight oxide on the end of these wires will result in a poor bond. Poor connections such as these would be difficult to locate and very difficult to correct. Although assembly of such a system can be mechanized, the basic optical grinding process is time consuming and costly.

Soldered Circuit Board - This interconnection scheme is similar to the Deposited Connections Approach with the exception that the interconnections are made on a separate

circuit board instead of the edges of the wafers. The circuit board used is a 1/64" double clad epoxy. Each board has a standard conductor pattern which consists of vertical lines on one side and horizontal lines on the opposite side. Connections between the two sides of the board are made by plated through holes.

The step-by-step procedure of assembly is described next. A master pattern consisting of parallel horizontal lines is prepared on a sheet of mylar. A similar pattern consisting of vertical lines is prepared on another sheet. Figure 2 shows these patterns. Registration marks are also provided on both sheets. Between the parallel lines, both sheets contain rows of circles, which are placed over the areas where the leads from the substrates are located. Another master pattern containing the locations for all of the holes is prepared on a metal plate. There are two types of holes. The larger holes will accept the leads from the substrates. The smaller holes are for the plated through interconnections which connect the front and back side of the circuit board.

When a given system is to be interconnected, the master connection pattern is first laid out on a specially prepared sheet of paper. Locations of the necessary plated through holes are determined. The master metal plate is placed over the double clad epoxy board and the registration holes are drilled. Next, the holes for the leads from the substrates are drilled

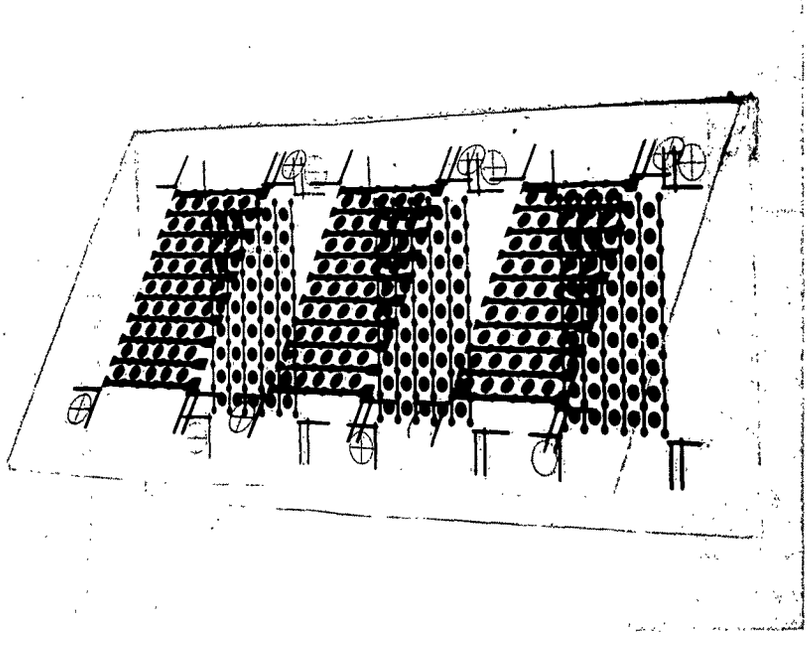

Figure 2. Mylar Pattern

and finally, the holes for the plated through connections are drilled. A typical board has two registration holes and only a handful of holes for the plated through connections. The majority of the drilling will be for the holes which will receive the leads. Fortunately, these holes are the same for each board regardless of the connection scheme; hence, they can be punched out to save time. The holes are then plated through.

The mylar master is programmed next. This is done by painting in areas with a special ink. Although a hand operation, it is fast and requires little skill. The mylar sheet is then placed over the drilled epoxy board. Standard printed circuit techniques are used to etch away the undesired copper areas. Upon completion of this step, the boards are ready for use. Figure 3 shows one side of the etched epoxy board. This is only a dummy board; hence, no programming holes or areas are visible.

Although the assembly procedure sounds complicated, it takes surprisingly little time. The most difficult part, the layout of the connection pattern, takes less than half an hour. Drilling of the holes is lengthy. However, the majority of these can be punched. The remainder of the functions are relatively easy and do not take much time.

This packaging approach allows for interconnection of inductors and filters in addition to the circuit wafer. Crystal filters which are . 625 inches wide can be obtained now.

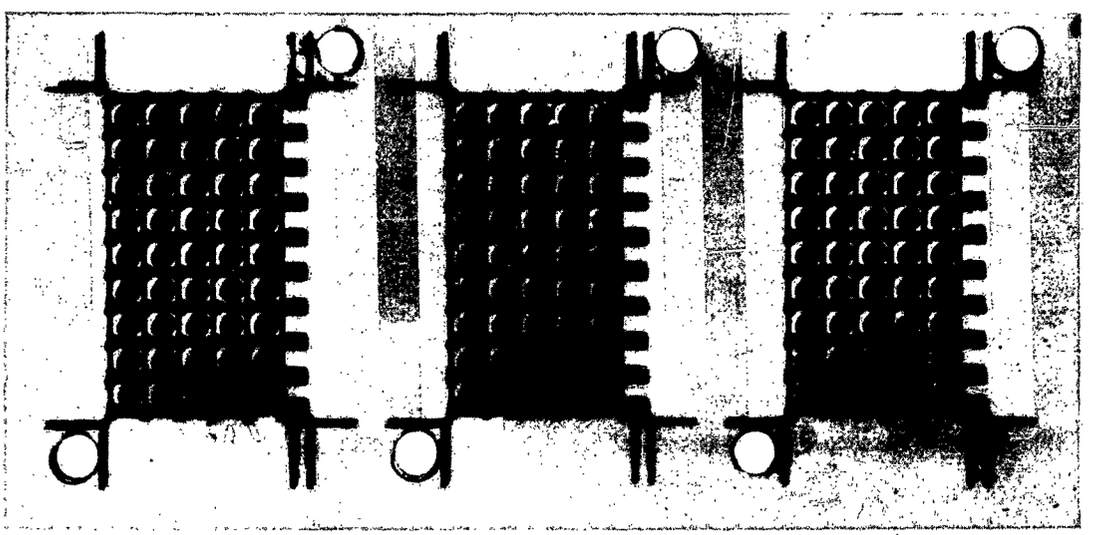

Figure 3. Interconnection Boards

In the near future, smaller size filters will be available. Inductors as small as 50 mils x 25 mils have been made. Commercially available inductors are slightly larger but are still small enough to use in these systems. These inductors would be packaged in a form factor compatible with the circuit wafers and interconnected in the same manner.

When the interconnection boards are finished the substrate leads are placed through the large holes. Next, the entire assembly is dip soldered in one operation. Figure 4 is a photograph of a complete digital divider. The module contains 4 flip-flops and 3 gates in a total volume of . 22 in.^{3}.

The interconnection method just described has several advantages over the methods described previously. Connections are made on two planes, one on each side of the epoxy board, which provides much flexibility in the design. The steps to prepare the connection pattern are the same as for printed circuits. Hence, existing facilities can be used. The majority of operations can be mechanized, therefore, assembly costs will be low. Repair of the modules, while not easy because a large number of joints must be unsoldered, is still feasible. This operation can be eased by using a specially shaped tip on the soldering iron.

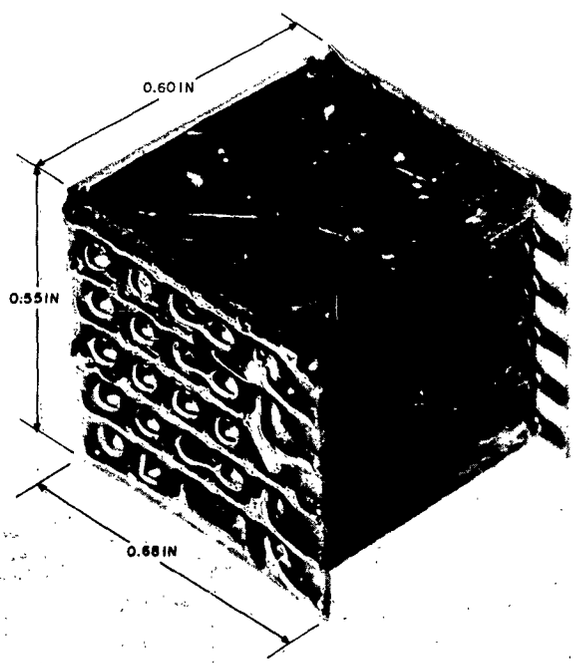

Figure 4. Digital Divider Module

3.2.3 Interconnection of Modules - The Amp Meca Approach

The modules which have been described in section 3.2.3 must now be interconnected to form a system. In addition to requirements of reliability, low cost and small volume is the need for easy replacement of the module. This last point makes the use of plug-in connectors mandatory.

The Amp Meca system is a packaging approach which allows one to interconnect circuits in three dimensions. It features individual cells which can be easily removed and replaced. Although not perfect, it is at the present time the best solution to the problem of economically connecting micro-circuit modules. In order to improve this system much further work would have to be done.

The three dimensional Meca cell serves the dual purpose of mechanical support and electrical contact. Figure 5 shows a typical cell. The cell has five solid faces and an open top. Along two sides are cut a number of vertical grooves. Metal contacts snap into these grooves. Each contact has a lip at the top which is attached to the circuitry inside the cell.

Figure 6 shows a system interconnected by means of Amp Meca. The side rails support Meca cells, provide contacts for the Meca cells, and support horizontal bus bars

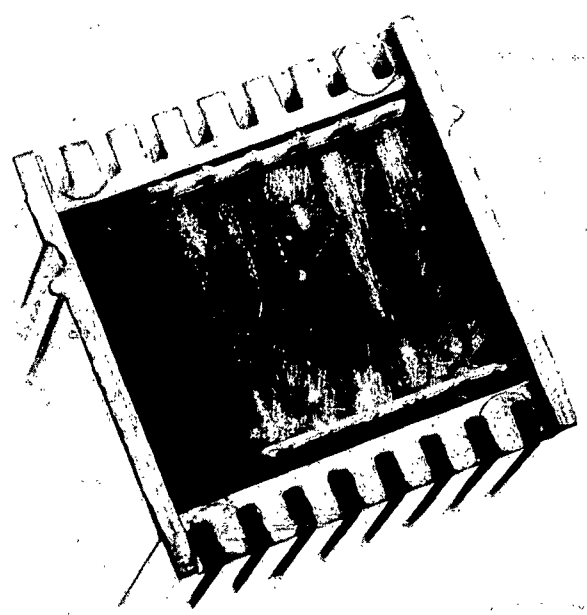

Figure 5. Amp Meca Cell

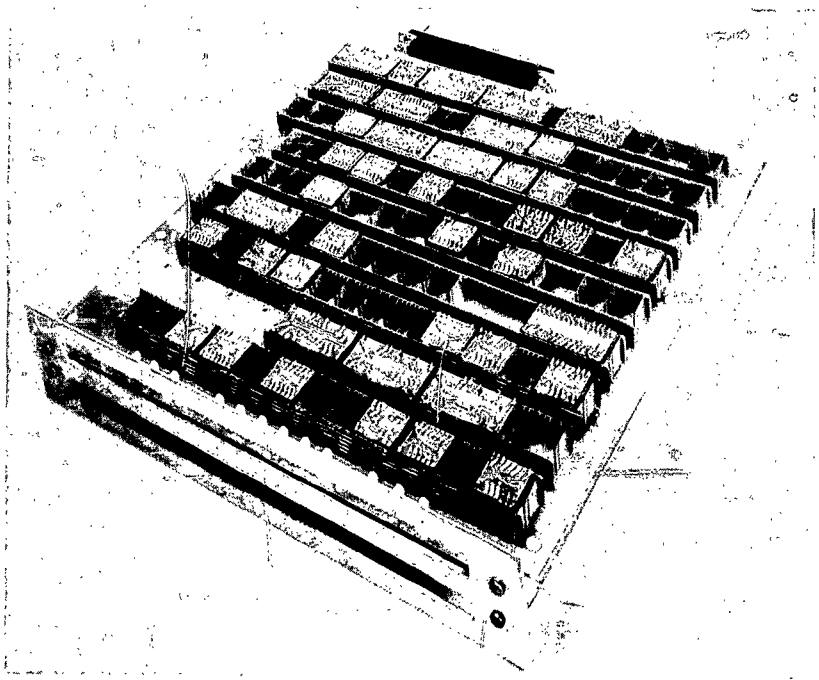

Figure 6. System Using Meca Connectors

which connect a cell to its neighbors. Each side rail has 5 bus bars; hence, up to 10 lines are available. Metal tines which slip into the contacts on a Meca cell are soldered to the side rails. They also fit into programmed holes in the mother board. Thus, connections between cells can be made either on the side rails or on the mother board. A more complete description of the Amp Meca system can be found in a paper presented at the Second International Electronic Circuit Packaging Symposium, 1961, entitled Maintainable Electronic Component Assemblies.

The Meca cells are available in a wide variety of sizes. Three basic grids are available: 50 mil, 100 mil and 200 mil. These dimensions refer to the center to center spacings of the vertical grooves cut into the Meca cells. The 100 mil grid of cells corresponds to the 100 mil thickness of the substrates, hence, that grid spacing will be used. Available sizes of cells are summarized below:

50 mil grid:

inside dimensions: .460" x .405" x .120"
outside dimensions: .500" x .485" x .310"

100 mil grid:

inside dimensions:

H = .51", .61", .71", .81", .91", 1.01"

W = .325", .425", .525", .625", .725", .825", .925", 1.025"

L = .17", .27", .37", .47", .57", .67", .77", .87", .97", 1.07", 1.17"

outside dimensions

H = .60", .70", .80", .90", 1.00", 1.10"

W = .59", .69", .79", .89", .99", 1.09", 1.19", 1.29"

L = .275", .375", .475", .575", .675", .775", .875", .975", 1.075", 1.175", 1.275"

200 mil grid: similar sizes are available

The Amp Meca approach has been chosen because it offers some very distinct advantages over conventional plug-in connectors. Each connection makes electrical contact in four separate points for maximum reliability. Contacts are made on two sides of a cell. Three other sides of the cell are used for support. Placing a retaining plate over the remaining face will insure that the cell cannot possibly work free. Even without a retaining plate, vibration tests have indicated that the cells will not work loose. Removing a cell from the circuit, on the other hand, is very easy.

In general, two types of conventional plugs are available. The first type can be easily removed but is not self supporting under vibration. The second type is self supporting but cannot be removed very easily. These characteristics are especially true if one considers only miniature connectors. The Meca connectors combine the advantages of both types, that is they are self supporting under vibration and can be easily removed.

Another advantage of the Amp Meca approach is its low cost. In a typical system, the cost of all connections including cells, contacts, tines and side rails is around one dollar per cell.

One problem with miniature connectors is that they are just now becoming available. Little test data is available. Furthermore, one cannot be certain that these will be accepted and will remain in production. The Meca approach has been in existance for several years now. A large amount of test data on these cells is presently available. Tests on contact resistance, electrical characteristics and thermal characteristics indicate that the cells will meet all of the requirements imposed on them by this system.

One question that may be raised at this point is the electrical coupling between the bus lines on the side rails. The capacitive coupling between adjacent lines is 1.1 pf per inch. In a small system such as this, no lines will run parallel to each other for any great distance. With careful layout, these parallel runs can be virtually eliminated. I-F amplifiers at 30 and 60 mc have been built using the Meca connection scheme. * Coupling between adjacent channels was below 60 db with no precaution for shielding or layout. Since these amplifiers were built with conventional components, their size was quite a bit larger than for the proposed system. In a small system, coupling is reduced drastically. Furthermore, the system can be laid out in a manner such that all critical lines will be separated by cells. Hence, coupling is not expected to be a serious problem.

3.3 CIRCUIT SPECIFICATIONS

3.3.1 General Remarks

The specifications given in this section have resulted from the following comprehensive program.

(1) A survey of the possible circuit approaches to use.

(2) Selection of the best circuit approach.

(3) Worst case circuit design considering component tolerances and active device parameter variations under worst case temperature conditions.

(4) Breadboard construction of the circuits in discrete form.

(5) Evaluation of the breadboard at room temperature conditions to verify design.

(6) Evaluation of the breadboards over the required temperature range with worst case loading and minimum input signal.

(7) Modification of the design as a result of deficiencies discovered in testing.

3.3.2 Test of Decade Divider

To characterize the Decade Divider, a complete set of tests were run on it. The tests were:

(1) Frequency, DC to max. frequency

(2) Temperature, 0°C to 100°C

* The few extra critical leads expected can be routed via subminiature coax, or strip lines.

(3) Loading, no load to 250Ω, 60 pf.

(4) Power Supply Voltage, 4 v. ± 5%

(5) Harmonic Analysis, Absolute Magnitude of Fundamental, and Noise Level at 20 mc.

Each of tests 1, 3, 4, and 5 was run individually at room temperature, after which the worst possible combination was tested to 100°C.

The operation of the divider, shown in the block diagram of figure 7 was tested from minimum to maximum frequency of stable operation at room temperature, no load conditions. The operable frequency range was from DC to 50 mc. The output pulse, 4 in figure 7, open circuit amplitude was 2.8 v. p. with a rise time of 10 nsec and a fall time of 5 nsec. With 20 pf. to ground and 1 k ohms to +4 v. on both 4 and its complement $\overline{4}$, the maximum frequency of operation at room temperature was 43.5 mc. Output pulse amplitude was 3.0 v. p. at 43.5 mc with a rise time of 20 nsec and a fall time of 8 nsec.

The capability of the divider, over the entire frequency range and 0°C to 100°C, was tested with varied degrees of loading. At 100°C and a load of 1k to +4v., 20 pf on both the pulse output and its complement, the maximum frequency of operation was 35 mcps. Pulse amplitude was 3.0 v. p. with a rise time of 20 nsec and a fall time of 8 nsec. With 250

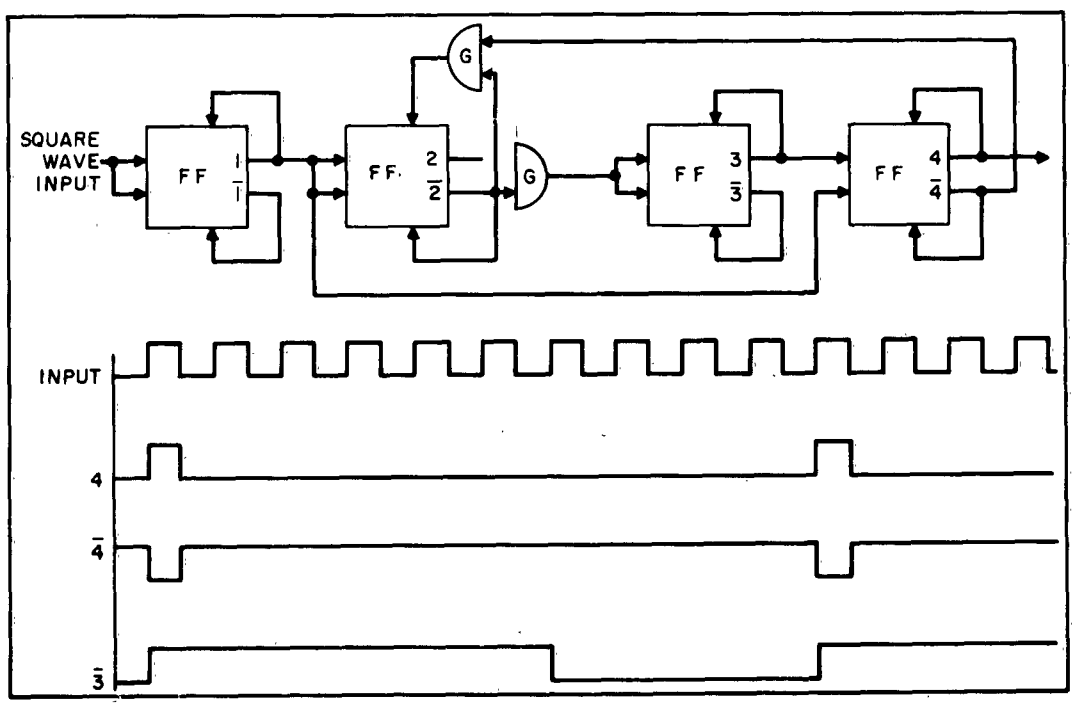

Figure 7. Block Diagram and Waveforms of Decade Divider

ohms to +4 v, and 60 pf. to ground on the pulse output, the pulse amplitude fell to 2.8 v. p. but the maximum frequency of operation remained 35 mcps.

The effect of 5% variation of power supply voltage was negligible under any loading conditions or any temperature of 0°C to 100°C.

The distortion content of the output pulse was measured using an Airmec Type 853 Wave Analyzer. Measurements were taken at room temperature and 20 mcps input, and both pulse output and its complement loaded with 1 k-ohms in parallel with 20 pf. Results are tabulated below.

f, mcps	2.0	4.0	6.0	8.0	10.0	12.0	14.0	16.0	18.0
db	0.0	+0.4	-2.5	-8.3	-18.5	-26.4	-15.4	-15.1	-17.7

Absolute magnitude of 2.0 mcps component = 468 mv. The noise level was at least 70 db down. The measurement level of the wave analyzer did not allow a measurement below 70 db.

To obtain more fundamental output and less higher harmonic content, the output $\overline{3}$ was examined. This output approaches a symetrical square wave much better than the final pulse output. Output $\overline{3}$ was loaded with 1k ohms in parallel with 20 pf. and the following measurements were taken.

f, mcps	2.0	4.0	6.0	8.0	10.0
db	0.0	-16.2	-16.3	-25.9	-23.2

Upon comparing the two tabulations, it is obvious that, insofar as harmonic content of the second and higher components is concerned, the output $\overline{3}$ is the more acceptable one.

Output $\overline{3}$ amplitude is 3.0 v. p. with a rise time of 10 nsec and a fall time of 7 nsec.

The minimum input level required to adequately drive the divider is 2.8 v. p. at 20 mc.

It may be noted that the decade divider supply voltage is 4 v. while the complete system is designed to operate from 6 v. No problems are anticipated in making the divider and system compatible, in that a simple resistor and zener diode will provide the required 4 v. from a 6 v. supply. This approach would also provide considerable electrical decoupling between the supply lines and the divider and will prevent the divider from triggering on false signals.

Decade Divider Specifications

Parameter		Min.	Design Center	Max.
Frequency Range	upper	30 mcps		
	lower			DC (0 cps)
Output Pulse Amplitude		2.8	3.0	3.2 volts
Pulse Rise Time (depends on loading)			15 nsec	
Pulse Fall Time		8	10	12 nsec
Input Voltage Required			2.8 volts	
Temperature	upper	100°C		
	lower			0°C
Power Supply Voltage			4 v	
Loading				250 to +4 v. 60 pf.
Pulse Fundamental Frequency (Amplitude)		300	400 mv.	
Noise Level (non-harmonic)				70 db

3.3.3 Digital Gate

The digital gate performs the NAND logical function. This is equivalent to the AND function and an inversion. The NAND function is called a universal function because any Boolean expression can be realized by using exclusively NAND elements. The gate operates in the following manner. When all of the inputs to the gate are high (positive voltage) the input diodes are back biased. Current flows through the 2 k resistor into the base and saturates the transistor. Hence, the output is in a low (ground) state. When one of the inputs is grounded, the corresponding input diode conducts. Point A is then clamped at about +0.9 volts. This potential is too low for current to flow into the base of the transistor, the transistor is turned off and the output then rises to the supply voltage. Grounding any of the remaining inputs does not change the output voltage in any manner. *

The gate has been designed for operation up to 30 mc under worst case conditions of temperature, loading, power supply variations and component variations. The DC design allows adequate margin for a fan in and fan out of 5. The base and collector current have been

* See footnote next page.

chosen to operate the gate at its most favorable power level, for maximum speed of operation. The 2N2369 has its maximum gain bandwidth product at a collector current of approximately 10 ma. This current corresponds to a fan out load of 2 gates.

Turn on time of the gate is under 5 nsec. Turn off time is dependent on the load. In general, the turn off time decreases as the load is increased. Storage time is very low because the capacitor across the two series diodes removes the stored minority carriers in the base.

In general, the gate is insensitive to component tolerances and temperature and power supply variations. This is due to the use of diodes as coupling elements. All of the components are in the range of values which can easily be realized by present microelectronic approaches. A number of such gates have been fabricated in thin film and the operating characteristics have been at least as fast as for conventional circuitry.

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* The NAND logical function arises because of the definition assumed here that a positive voltage represents a logical 1 and ground represents a logical 0. Had the opposite definition been assumed, the NOR logical function would be performed. The truth tables serves to explain the action.

positive voltage = 1
ground = 0

A	B	C	X
1	1	1	0
0	1	1	1
1	0	1	1
0	0	1	1
1	1	0	1
0	1	0	1
1	0	0	1
0	0	0	1

thus $X = \overline{A\,B\,C}$
or the NAND or Stroke function

ground = 1
positive voltage = 0

A	B	C	X
1	1	1	0
0	1	1	0
1	0	1	0
0	0	1	0
1	1	0	0
0	1	0	0
1	0	0	0
0	0	0	1

thus $X = \overline{A+B+C}$
or the NOR function

Thus the same gate can be used to perform NAND or NOR functions, depending on the definition of the logic levels.

Digital Gate Design Characteristics (see also figure 8)

Requirement	Minimum	Design Center	Maximum
Input Signal Frequency	0 cps.		30 mc.
Input Signal Level			
Gate On	+1. 8 volts		
Gate Off			+. 8 volts
Output Signal Level			
Gate On			. 50 volts
Gate Off		6 volts	
Power Supply	5. 4 volts	6 volts	6. 6 volts
Temperature Range			
Upper	+65°C		
Lower			0°C

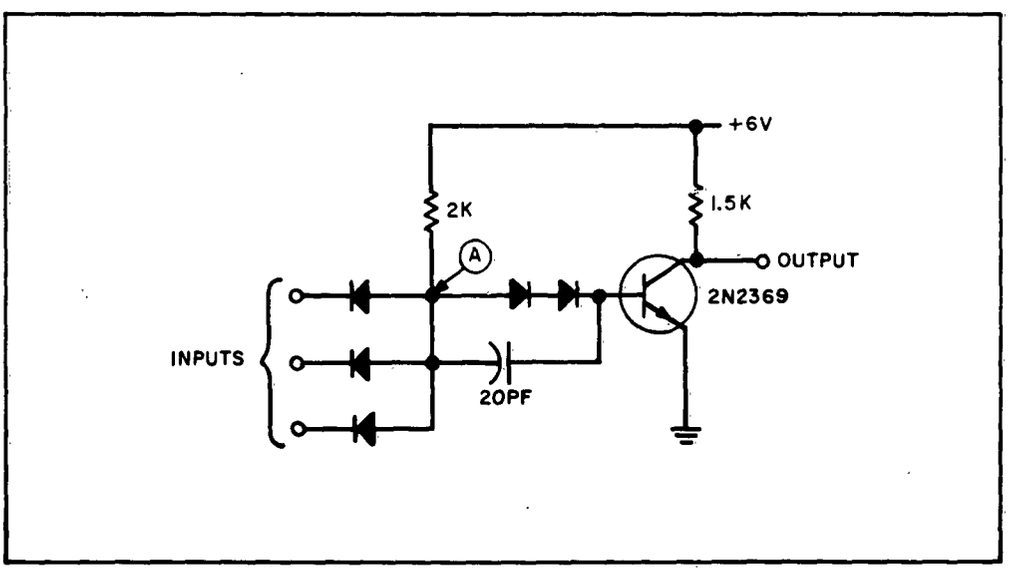


Figure 8. Digital Gate

3.3.4 Universal Amplifier

3.3.4.1 Selection of Transistor

Several factors were of importance when selecting a transistor for the Universal Amplifier. One factor was whether or not the particular transistor was available in microminiature form for placement on a thin film wafer. Other important factors include transistor dissipation, input and output impedance levels, frequency response, performance over a temperature range, and price. Transistor 2N2369 has several characteristics which make it desirable for use in the thin film block. This transistor was designed for use in both linear and non-linear operation; thus making it very flexible. It has a typical gain bandwidth product of 650 mc which eanbles it to be used over a wide frequency range. The input impedance is high at frequencies below 50 mc (typically 1k) which enables it to be driven easily. Below 50 mc the output impedance is large enough to enable the impedance matching network to have a loaded Q of 10 or better. This transistor comes in microminiature form so that it can be mounted on a thin film wafer. Under maximum operating conditions, the transistor will dissipate 60 milliwatts which is only 1/2 of the maximum total dissipation allowed on a single wafer. Furthermore, this transistor performs well over a temperature range from -55° C to 100° C. When used as an amplifier, it performed very satisfactorily from -10° C to 100° C. Also, the transistor is priced very reasonably now, and the manufacturer expects that it will become popular and, therefore, the price should come down even more in the future.

One disadvantage of the 2N2369 is that the microminiature package comes with aluminum leads which make soldering difficult. Also, the leads are very brittle. The package can be worked with however, and it is expected that an improved package will become available.

3.3.4.2 Stability Considerations

When an active device is used as an amplifier, there are certain conditions under which the amplifier will become unstable and will oscillate. This problem is most pronounced when both the input and output to the amplifier are tuned to the same frequency. This condition is known as conjugate matching. Figure 9 illustrates the general case. Referring to the figure, if $B_G = -B_i$ and $B_L = -B_0$ the amplifier is conjugate matched.

It has been shown* that a stability factor ρ, (refer to figure 9 for meaning of parameters) defined as $\rho = 2\,(g_{11} + G_G)\,(g_{22} + G_L)\,/M\,(1 + \cos 0)$, can be used to determine

* "Designing Unneutralized Tuned Transistor Amplifiers by Use of a Westinghouse Developed Test Set" R. M. Frazier, Westinghouse Electronics Division - Report No. 306.6, March 1958.

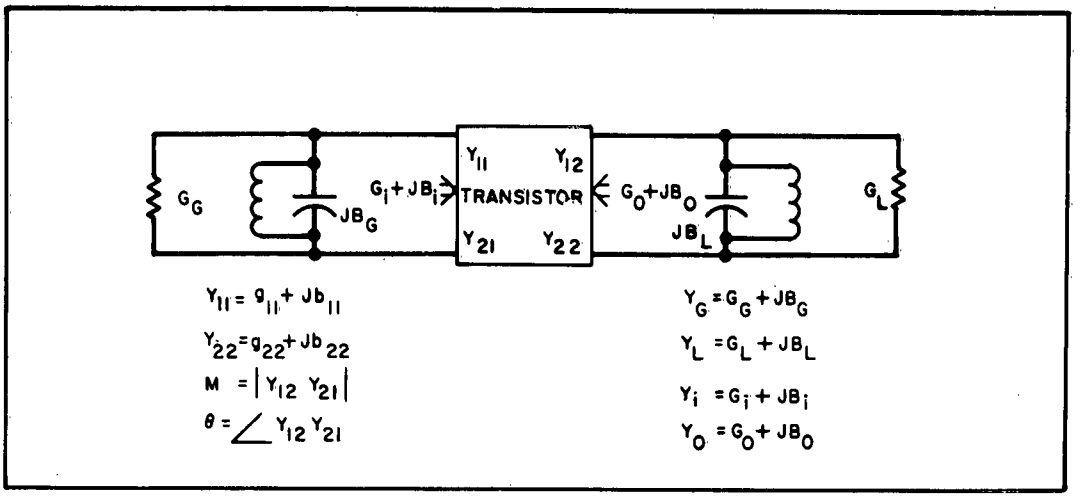


Figure 9. Linear Amplifier

if an amplifier will oscillate. If $\rho < 1$ the maximum possible gain of the circuit is infinite and the amplifier oscillates. If $\rho > 1$ the maximum possible gain is finite and the circuit is stable.

From the equation defining ρ it can be seen that the worst case occurs when $G_G=G_L=0$. If ρ is greater than 1 under those conditions, the circuit will be stable for all generator and load impedances.

It should be pointed out that since ρ is a function of the Y parameters of the active device, ρ will be a function of bias point, temperature, and frequency.

The Y parameters for transistor 2N2369 are given from 50 mc to 500 mc. If it is assumed that $G_G=G_L=0$, it is possible to plot ρ as a function of frequency for the 2 N2369. Figure 10 shows the variation of ρ with frequency. At frequencies from 350 mc to 450 mc, ρ is less than 1, meaning that the transistor is inherently unstable over that frequency range. If it is to be used as an amplifier over that frequency range, it would be necessary to increase G_L and G_G. At frequencies below 350 mc down to 50 mc, ρ is greater than 1 and the device is stable. The graph shows that ρ is decreasing rapidly below 100 mc. It appears that from the graph that below 50 mc ρ might become quite close to 1.

The amplifier was first breadboarded with no feedback resistance in the emitter lead. With this configuration, the amplifier was stable from 100 kc to 30 mc even when conjugate matched. However, when the emitter resistance was added, the amplifier became potentially unstable at 10 to 20 mc. When the amplifier with the emitter resistor was conjugate

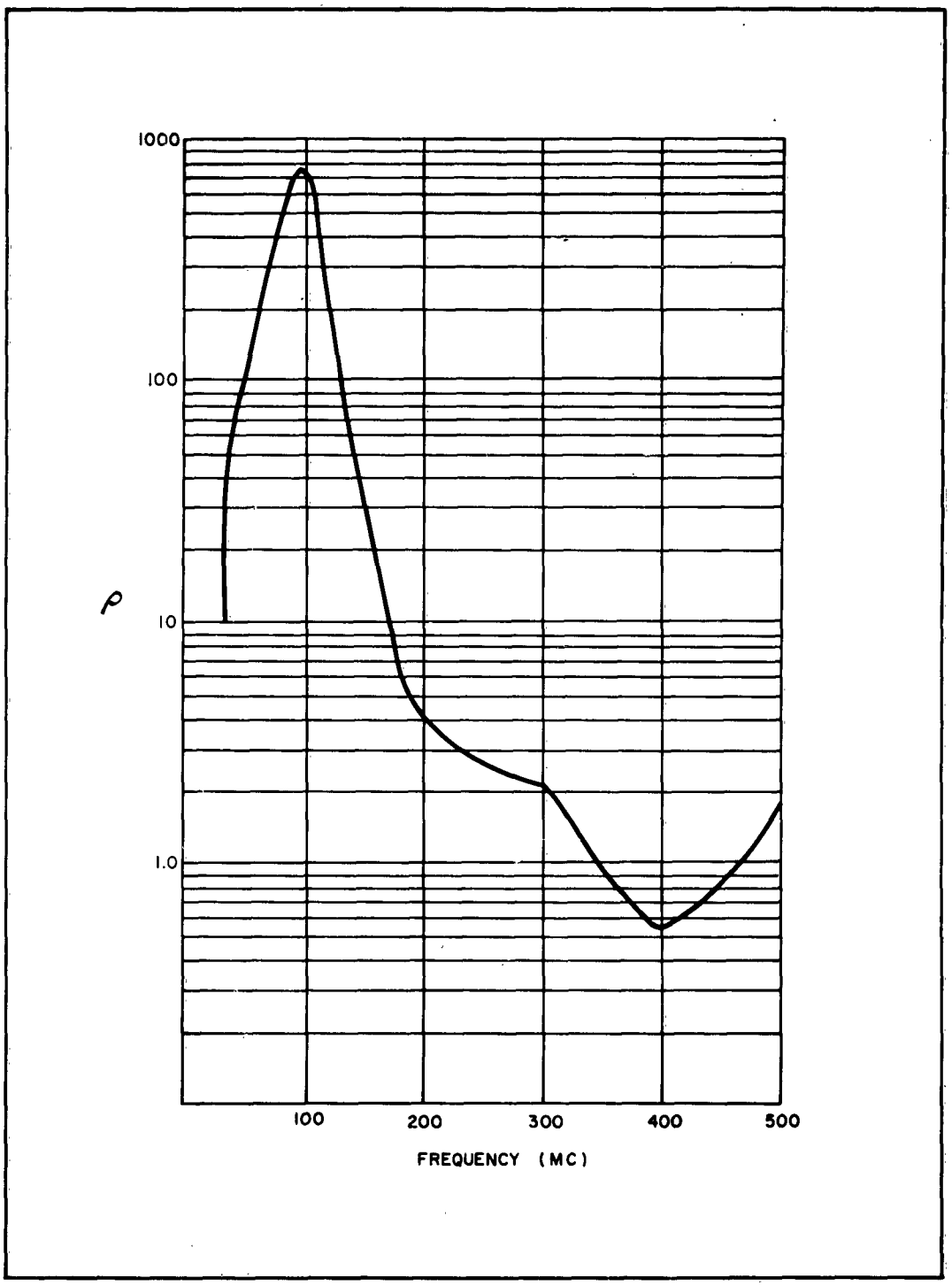


Figure 10. Stability (ρ) as a Function of Frequency

matched, it would oscillate. The reason for this can be seen by examining the equation defining ρ . With the emitter resistor added, the input and output impedances are increased which means g_{11} and g_{22} are decreased. Since ρ was already quite close to 1, the addition of the emitter resistor caused it to go below 1.

There may be certain applications where the input capacitance of the Universal Amplifier is high. The amplifier however can be driven in one of the following ways:

1. By a preceeding tuned amplifier employing a pi network, where the input capacitance becomes part of that network. See paragraph 3. 3. 4. 5.
2. For marginal cases, partial conjugate can be used to lower the reactive capacitance to a convenient value for the preceeding stage to drive it. This method introduces an inductor, whose unloaded Q requirement is not critical.
3. For extreme cases, where very little capacitance is required at the input, an emitter follower preceeding the amplifier is a solution.

3. 3. 4. 3 Load Line

The collector of the Universal Amplifier works into a resistive load. The magnitude of this load is important as far as voltage gain and power gain is concerned. The low frequency voltage gain(V.G.), for instance, is given by*

$$V.G. = (-h_{21}/h_{11})/\left[G_{in}+h_{22}(1-h_{12}h_{21}/h_{11}h_{22})\right]$$ where h_{11}, h_{12}, h_{21}, and h_{22} are the standard hybrid parameters for a "black box". Upon examining this equation. it can be seen that the maximum voltage gained occurs when $G_{in} = 0$.

The expression for power gain is given by*

$$P.G. = (h^2_{21}/h_{11}h_{22})\,(1/1+h_{22}R_{in})\left[1/\left(1 - \frac{h_{12}h_{21}}{h_{11}h_{22}} + \frac{1}{h_{22}R_{in}}\right)\right]$$

where R_{in} is the resistance seen by the collector of the transistor.

This equation shows that the power gain is zero for R_{in} equal to either zero or infinity. Thus there is some R_{in} where the power gain will be a minimum.

* "Handbook of Semiconductor Electronics", Lloyd P. Hunter, McGraw-Hill Book Co., 1956, P. 11-22.

The voltage gain and power gain are not the only criterion for choosing the load seen by the collector. It is also important that the load be chosen so that the parameter values for the impedance matching network are practical. Furthermore, the finite Q of the inductor L in the impedance matching network places an upper limit on the load seen by the collector.

Figure 11 shows the variation of power gain with different loads when the 2N2369 is used in the Universal Amplifier. Note that the power gain peaks at a load of approximately 1 k. A typical gain for this load is 30 db over the frequency range of interest (100 kc to 20 mc). Furthermore, an R_{in} of 1 k results in large values for the capacitors C_1 and C_2 (see figure 12) and small values for the inductor L. The values for C_2 are particularly large which means that any capacitance associated with the final load will not affect the tuning. Also the small values for L are advantageous as far as microminiaturization is concerned.

3.3.4.4 Negative Feedback

The use of negative feedback in the R-F Amplifier and Multiplier was incorporated primarily to reduce the spread in gain with different transistors.

Another advantage resulting from this is the increase in input resistance and reduction of input capacitance.

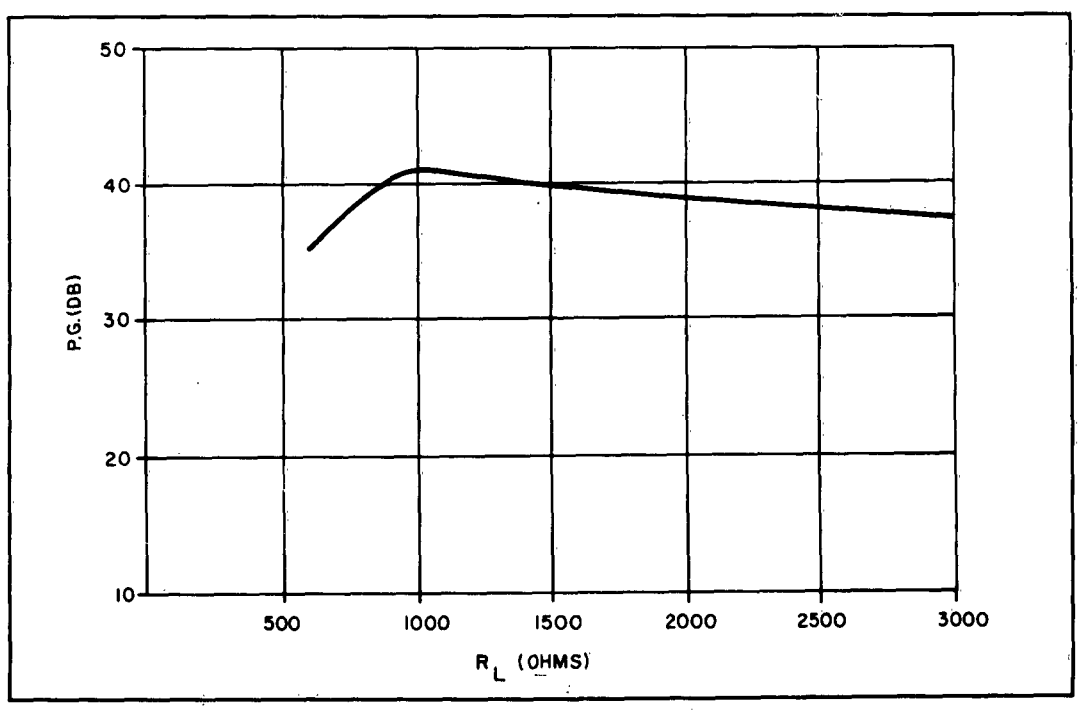


Figure 11. Power Gain as a Function of R_{in}

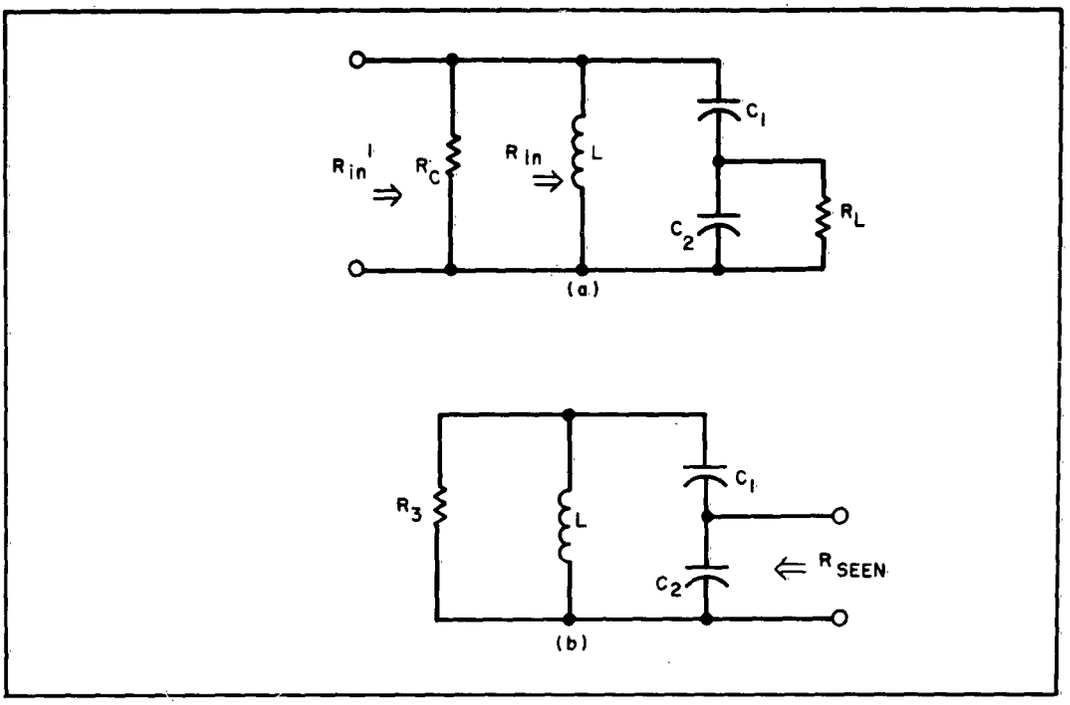


Figure 12. Impedance Matching Network

The following tabulation shows typical values for input resistance, input capacitance, and variation of output voltage for amplifier using transistor 2N2369 with and without feedback. The percentage in output voltage variation is given for a group of six transistors taken at random. Their performance was recorded at each frequency. The table shows the percentage variation in output voltage.

Without Feedback				With Feedback		
Frequency	Input R	Input C	% output voltage variation W. R. T. Transistors	Input R	Input C	% output voltage voltage W. R. T. Transistors
100 Kc	630	480 pf	21%	1. 3K	140 pf	4. 2%
1 Mc	460	370 pf	22%	870	180 pf	7%
10 Mc	170	230 pf	28%	3K	108 pf	4. 2%
20 Mc	73	160 pf	20%	2K	41 pf	5%

Figure 13 shows the variation of power gain with frequency with feedback and without feedback.

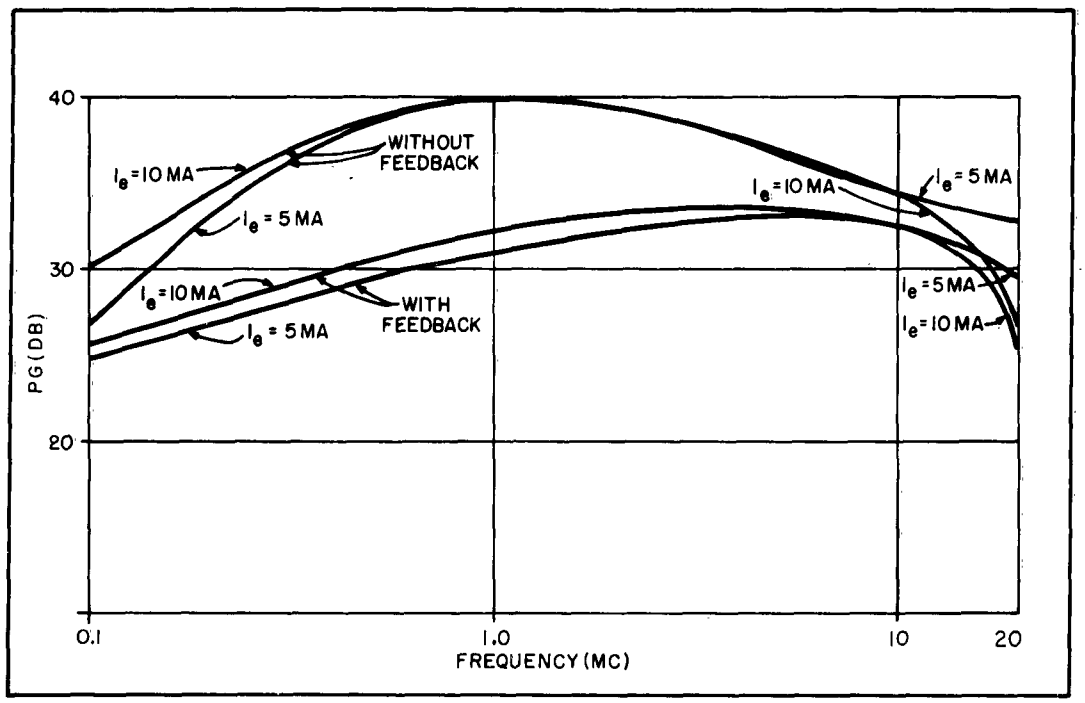


Figure 13. Power Gain Versus Frequency

Without feedback, the voltage gain of the Universal Amplifier is quite sensitive to emitter current. Figure 14 illustrates the improvement which results from feedback.

The improvement in linearity is shown in figure 15.

3. 3. 4. 5 Pi Network Design

The type of network used in the output of the Universal Amplifier is shown in figure 12. This network, when tuned to resonance, presents a resistive load to the collector of the transistor.

To determine the correct value for L, C_1, and C_2, it is necessary to know the load R_L, and the reflected resistance R_{in}. The values for X_L, X_{C1}, and X_{C2} are calculated from*

$$X_L = \left| R_{in} R_L \sin B / \left(R_L \cos B - \sqrt{R_{in} R_L} \right) \right| , \quad X_{C1} = \sqrt{R_{in} R_L} \sin B, \text{ and}$$

* "Radio Engineers Handbook", Frederick E. Terman, McGraw-Hill Book Co., 1943.

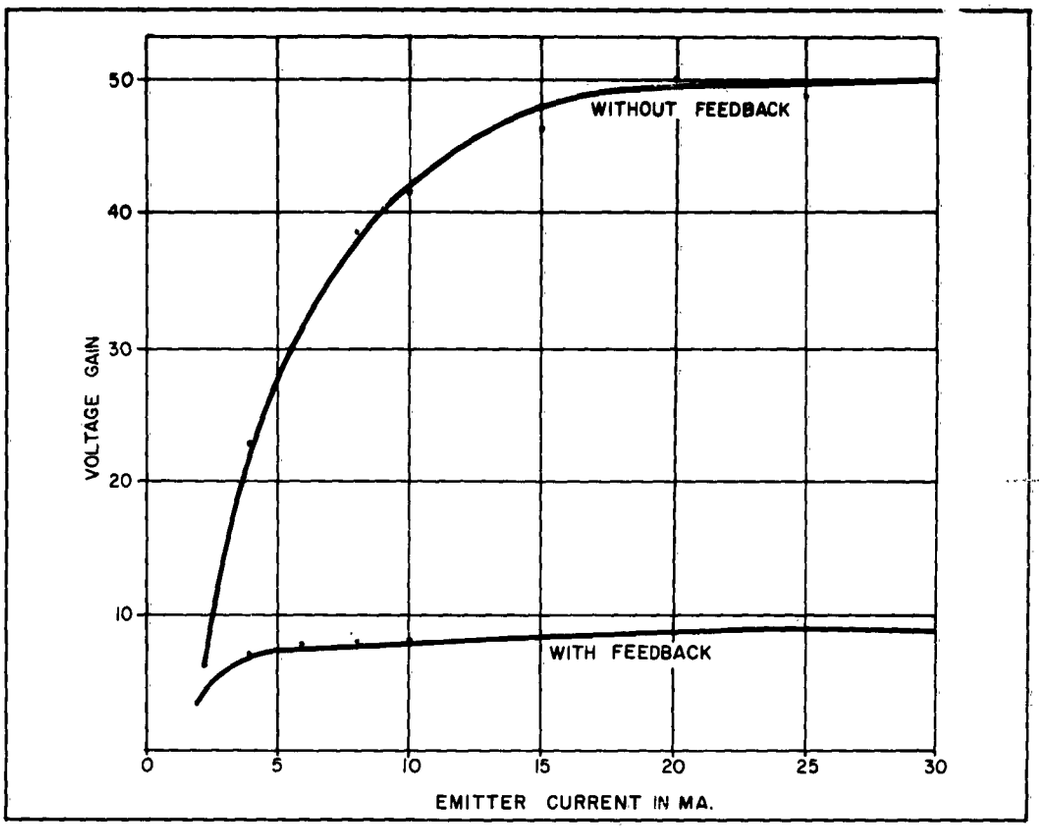


Figure 14. Voltage Gain as a Function of Ic

$X_{C2} = \left| R_{in} R_L \sin B \Big/ \left(R_{in} \cos B - \sqrt{R_{in} R_L} \right) \right|$. In these equations B is the angle between the input and output voltages. In general, smaller angles result in higher loaded Qs. This can be seen from the formula for the loaded Q. $Q_L = \frac{R_P}{X_L}$ where R_P is the parallel combination of the transistor output resistance R_o, the resistance R_c due to the finite Q of the coil, and the reflected resistance R_{in}. Q_L will increase with decreasing X_L and X_L decreases with decreasing B. Angle B of below 10° is satisfactory. If the loaded Q for a given B is too low, a lower value of B must be chosen and the calculations for X_L, X_{C1}, and X_{C2} will have to be repeated.

The actual resistance seen by the transistor will not be the desired R_{in} because of the finite Q of the coil. The coil is shunted with a resistance R_c euqal of $Q_u X_L$ where Q_u is the unloaded Q of the coil. The transistor sees the parallel combination of R_{in} and R_c.

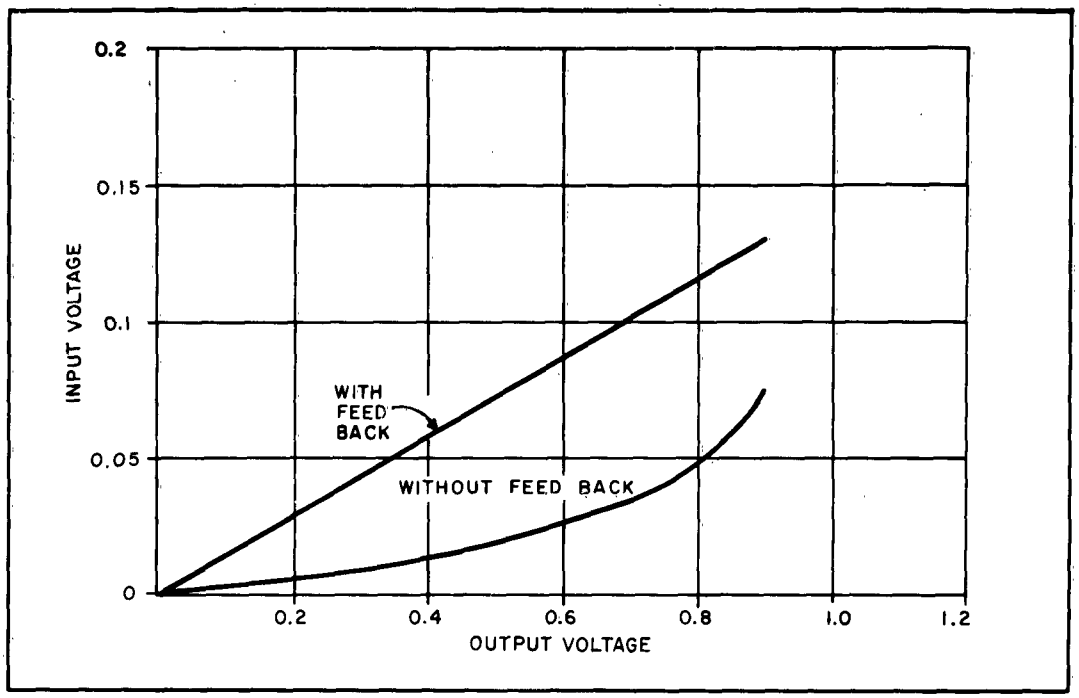


Figure 15. Amplifier Linearity

If the resistance R_c is not 10 times larger than R_{in}, then it may be necessary to calculate X_L, X_{C1}, and X_{C2} by accounting for the Q of the coil. The coil Q must be known to within ±5% for this method to work. Refer to Appendix B, part 1, for the equations defining X_L, X_{C1}, and X_{C2} by accounting for the Q of the coil.

There are certain applications, for instance when the amplifier load is a crystal filter, where the resistance looking back from the load into the network must be equal to the load resistance. This resistance is given by

$$R_{seen} = \left[R_3^2 \left(1 - \frac{X_L}{X_{C1}}\right)^2 + X_L^2 \right] \Big/ R_3 \left(\frac{X_L}{X_{C1}}\right)^2$$

(refer to Appendix A, part 2, for derivation) where R_3 is the equivalent resistance shunting the coil. The resistance R_3 consists of the output resistance of the transistor in parallel with the resistance R_c due to the Q of the coil. If R_{seen} is to be equal to the load resistance R_L, it is necessary for R_3 to be equal to R_{in}.

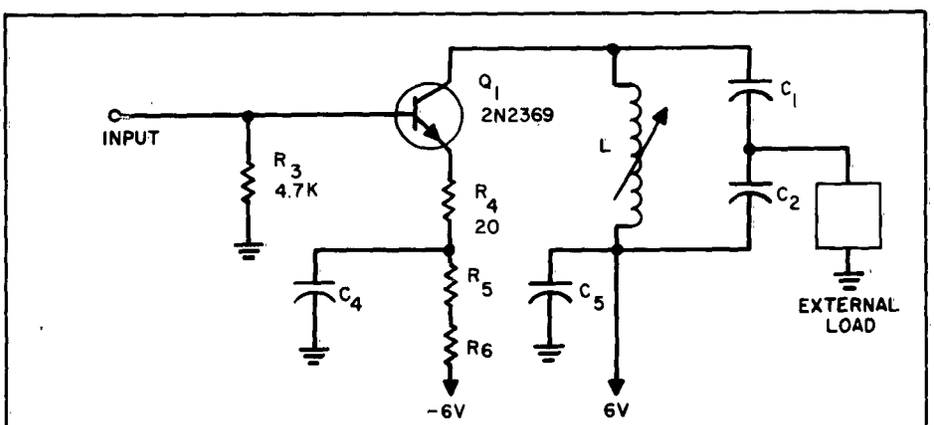
3. 3. 4. 6 Design Characteristics of Basic Circuits

Figure 16 through 19 show the schematic of the basic analog circuits; R-F Amplifier, frequency multiplier, emitter followed and mixer. Tables 1 through 12 shows their design characteristics for collector currents of 5 and 10 milliamperes.

Mixers are shown for one collector current value only because of the special non-linear operation of this device.

Design characteristics for R-F Amplifiers are shown for input frequencies of 100 kc, 1 mc, 10 mc and 20 mc. Design characteristics for multipliers are shown for input frequencies of 1, 2, and 4 mc, and multiplication factors of 2, 4, and 5, supplying outputs from 2 to 20 mc.

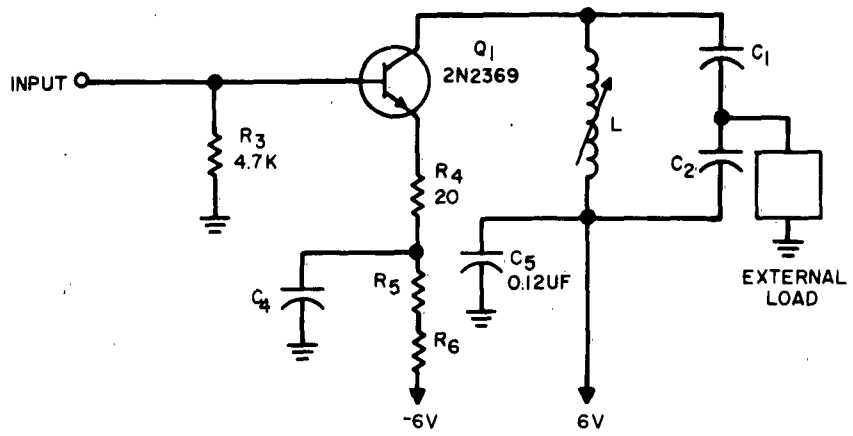
The emitter follower is for wideband operation. Its input level, input resistance and input capacitance are dependent on output load.



I_e	R_5	R_6
5 MA.	560	560
10 MA.	560	0

FREQ.	C_4	C_5	C_1	C_2	L
100 KC	1 UF	1UF	30,000 PF	67,000 PF	108 UH
1 MC	0.2 UF	0.12 UF	3,000 PF	6800 PF	10.8 UH
10 MC	0.12 UF	0.12 UF	290 PF	680 PF	1.1 UH
20 MC	0.12 UF	0.12 UF	150 PF	330 PF	0.545 UH

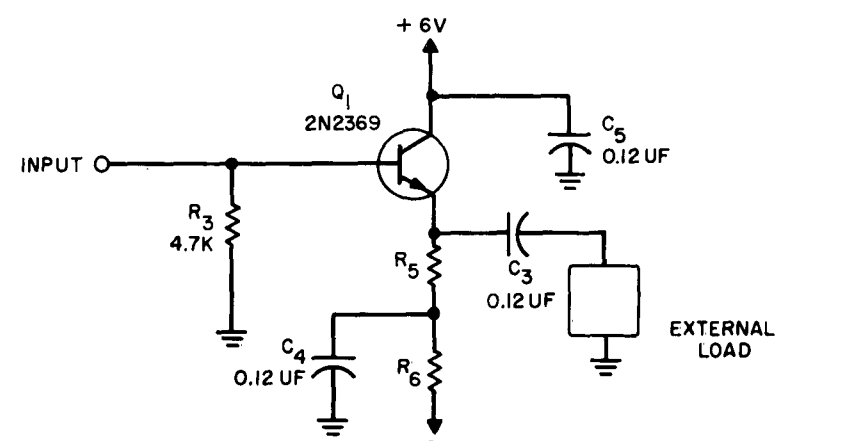
Figure 16. R-F Amplifier



I_e	R_5	R_6
5 MA	560	560
10 MA	560	0

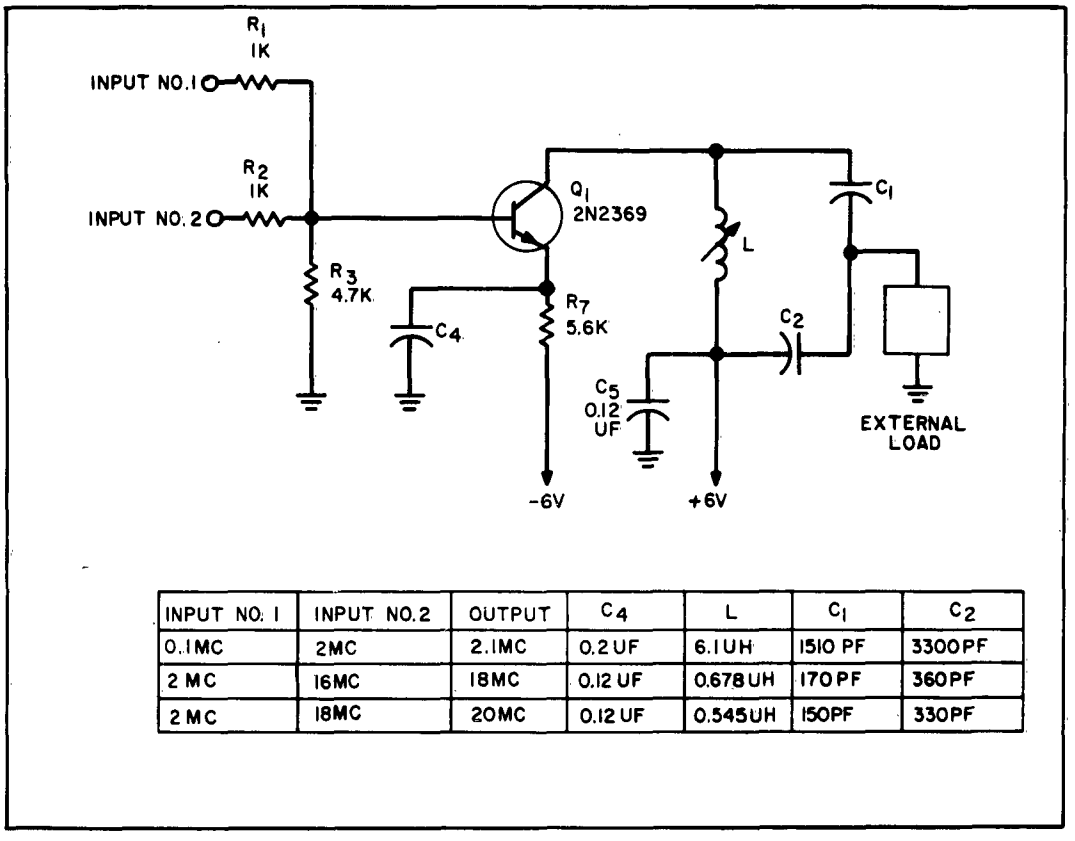
INPUT FREQ.	OUTPUT FREQ.	C_4	C_1	C_2	L
1MC	2 MC	0.2UF	1510 PF	3300PF	6.1 UH
2 MC	4 MC	0.12 UF	750PF	1510PF	3 UH
4 MC	16 MC	0.12 UF	195 PF	405 PF	0.765UH
4 MC	20MC	0.12 UF	150 PF	330 PF	0.545UH

Figure 17. Multiplier



I_e	R_5	R_6
5MA	560	560
10MA	560	0

Figure 18. Emitter Follower



INPUT NO. 1	INPUT NO.2	OUTPUT	C_4	L	C_1	C_2
0.1MC	2MC	2.1MC	0.2 UF	6.1UH	1510 PF	3300PF
2 MC	16MC	18MC	0.12 UF	0.678UH	170PF	360PF
2 MC	18MC	20MC	0.12 UF	0.545UH	150PF	330PF

Figure 19. Mixer

Table 1 - Design Characteristics

For 100 Kc Amplifier
5 and 10 ma Operation

Requirements 1/	Minimum	Design Center 2/	Maximum 2/
Input Level			100mV/190mV
Input Capacitance		140 picofarads	
Input Resistance		1.3 k ohms	
Output Amplitude			0.5v/1.0v
Voltage Gain		4.7/5.3	
Power Gain		24/25 db	
Output Voltage variation (for ±5% supply voltage change)			1%
Operating Temperature			
Upper Limit	100°C		
Lower Limit			-10°C
Linearity (for 0.005 to 0.150V input range)			6%/2%
Power Supplies			
#1		+6 volts	
#2		-6 volts	
Current Consumption		5 ma/10 ma	

1/ For an external load resistance of 100 Ω in parallel with 100 picofarads. Q of tuned circuit is 10±1, and at resonance offers a resistive load of 1K ohms to the transistor.

2/ When two figures are shown, upper figure is for 5 MA, lower figure for 10 MA collector current.

Table 2 - Design Characteristics

For 1 Mc Amplifier
5 and 10 ma Operation

Requirements 1/	Minimum	Design Center 2/	Maximum 2/
Input Level			105mV/105mV
Input Capacitance		180/184 picofarads	
Input Resistance		1.53kΩ/870Ω	
Output Amplitude			1.0V/1.0V
Voltage Gain		10/11.7	
Power Gain		31 db/32 db	
Output Voltage variation (for ± 5% supply voltage change)			1%
Operating Temperature			
Upper Limit	100°C		
Lower Limit			-10°C
Linearity (for 0.005 to 0.150V input range)			±1%/±6%
Power Supplies			
#1		+6 volts	
#2		-6 volts	
Current Consumption		5 ma/10 ma	

1/ For an external load resistance of 100Ω in parallel with 100 picofarads. Q of matching circuit is 10±1, and at resonance offers a resistive load of 1K ohms to the transistor.

2/ When two figures are shown, upper figure is for 5 ma, lower figure for 10 ma collector current.

Table 3 - Design Characteristics

For 10 Mc Amplifier
5 and 10 ma Operation

Requirements 1/	Minimum	Design Center 2/	Maximum 2/
Input Level			120mV/120mV
Input Capacitance		96/110 picofarads	
Input Resistance		3.8K ohms/3K ohms	
Output Amplitude			0.85V/1.0V
Voltage Gain		7.5/8.3	
Power Gain		33 db/ 33 db	
Output Voltage variation (for ± 5% supply voltage change)			1%
Operating Temperature			
Upper Limit	100°C		
Lower Limit			-10°C
Linearity (for 0.005 to 0.150V input range)			6%/2%
Power Supplies			
#1		+6 volts	
#2		-6 volts	
Current Consumption		5 ma/10 ma	

1/ For an external load resistance of 100Ω in parallel with 50 picofarads. Q of matching circuit is 10±1, and at resonance offers a resistive load of 1K ohms to the transistor.

2/ When two figures are shown, upper figure is for 5 ma, lower figure for 10 ma collector current.

Table 4- Design Characteristics

For 20 Mc Amplifier
5 and 10 ma Operation

Requirements 1/	Minimum	Design Center 2/	Maximum 2/
Input Level			125mv/125mv
Input Capacitance		42 picofarads	
Input Resistance		2K ohms	
Output Amplitude			0.88/0.98v
Voltage Gain		6.8/7.5	
Power Gain		29 db/ 30 db	
Output Voltage variation (for ± 5% supply voltage change)			1%
Operating Temperature			
Upper Limit	100°C		
Lower Limit			-10°C
Linearity (for 0.005 to 0.150V input range)			4%/2%
Power Supplies			
#1		+6 volts	
#2		-6 volts	
Current Consumption		5 ma/10 ma	

1/ For an external load resistance of 100Ω in parallel with 25 picofarads. Q of matching circuit is 10±1, and at resonance offers a resistive load of 1k ohms to the transistor.

2/ When two figures are shown, upper figure is for 5 ma, lower figure for 10 ma collector current.

Table 5 - Design Characteristics

For Multiplier x 2
2 Mc Output
For 5 ma and 10 ma Operation

Requirements 1/	Minimum	Design Center 2/	Maximum 2/
Input level		0.35v/0.66 volts	
Input Capacitance		17/19 picofarads	
Input Resistance		2.2/1.7K ohms	
Output amplitude			0.57/1.1 volts r.m.s.
Power Gain		17.6 db/ 16.8 db	
Output Voltage Variation (for ±5 percent supply voltage change)			1%
Operating temperature			
Upper Limit	100°C		
Lower Limit			-10°C
Power Supplies			
#1		+6 volts	
#2		-6 volts	
Current Consumption		5 ma/10 ma	

1/ For an external load of 100 ohms in parallel with 100 picofarads. Q of matching circuit is 10 ± 1 and at resonance offers a resistive load line of 1k ohms to the transistor.

2/ When two figures are shown, upper figure is for 5 ma, lower figure for 10 ma collector current.

Table 6 - Design Characteristics

For Multiplier x 2
4 Mc Output
For 5 ma and 10 ma Operation

Requirements 1/	Minimum	Design Center 2/	Maximum 2/
Input level		1.0V/0.9V	
Input Capacitance		14/16 picofarads	
Input Resistance		2.8K ohms/2.3K ohms	
Output amplitude			1.2 Volts/1.5 volts r.m.s.
Power Gain		16 db/17.7 db	
Output Voltage Variation (for ±5 percent supply voltage change)			1%
Operating temperature			
Upper Limit	100°C		
Lower Limit			-10°C
Power Supplies			
#1		+6 volts	
#2		-6 volts	
Current Consumption		5 ma/10 ma	

1/ For an external load of 100 ohms in parallel with 50 picofarads. Q of matching circuit is 10 ± 1 and at resonance offers a resistive load line of 1k ohms to the transistor.

2/ When two figures are shown, upper figure is for 5 ma, lower figure for 10 ma collector current.

Table 7 - Design Characteristics

For Multiplier x 4
16 Mc Output
For 5 ma and 10 ma Operation

Requirements 1/	Minimum	Design Center 2/	Maximum 2/
Input level		1.0V/0.8 volts	
Input Capacitance		13/14 picofarads	
Input Resistance		2.6K ohms/2.1K ohms	
Output amplitude			0.27V/0.27 volts r.m.s.
Power Gain		2.7 db/3.5 db	
Output Voltage Variation (for ± 5 percent supply voltage change)			1%
Operating temperature			
Upper Limit	100°C		
Lower Limit			-10°C
Power Supplies			
#1		+6 volts	
#2		-6 volts	
Current Consumption		5 ma/6 ma	

1/ For an external load of 100 ohms in parallel with 50 picofarads. Q of matching circuit is 10 ± 1 and at resonance offers a resistive load line of 1K ohms to the transistor.

2/ When two figures are shown, upper figure is for 5 ma, lower figure for 10 ma collector current.

Table 8 - Design Characteristics

For Multiplier x 5
20 Mc Output
For 5 ma and 10 ma Operation

Requirements 1/	Minimum	Design Center 2/	Maximum 2/
Input level		0.77V/1.0 volts	
Input Capacitance		13/14 picofarads	
Input Resistance		2.6K/2.1K ohms	
Output amplitude			0.16/0.33 volts r.m.s.
Power Gain		0.5 db/3.6 db	
Output Voltage Variation (for ± 5 percent supply voltage change)			1%
Operating temperature			
Upper Limit	100°C		
Lower Limit			-10°C
Power Supplies			
#1		+6 volts	
#2		-6 volts	
Current Consumption		5 ma/10 ma	

1/ For an external load of 100 ohms in parallel with 50 picofarads. Q of matching circuit is 10 ± 1 and at resonance offers a resistive load line of 1K ohms to the transistor.

2/ When two figures are shown, upper figure is for 5 ma, lower figure for 10 ma collector current.

Table 9 - Design Characteristics for Emitter Follower

5 and 10 ma Operation

Requirements	Minimum	Design Center	Maximum 1/
Input Level:			
for 50 ohms load			0.19 volts/0.36V
for 100 ohms load			0.33 volts/0.65V
for 500 ohms load			1.25 volts/1.9V
Input Capacitance:			
for 50 ohms load		14 picofarads	
for 100 ohms load		10 picofarads	
for 500 ohms load		8 picofarads	
Input Resistance:			
for 50 ohms load		2.2K ohms	
for 100 ohms load		2.7K ohms	
for 500 ohms load		3.8K ohms	
Voltage Gain:			
for 50 ohms load			0.83
for 100 ohms load			0.91
for 500 ohms load			0.96
Output Impedance:			
for 200 ohms generator			15 ohms
for 1K ohms generator			20 ohms
Frequency Response:			
± 0.5 db	50 KC		greater than 50 MC
Operating Temperature			
Upper Limit	100°C		
Lower Limit			-10°C
Power Supplies			
#1		+6 volts	
#2		-6 volts	
Current Consumption		5 ma/10 ma	

1/ For an external load of 100 ohms in parallel with 50 picofarads. Q of matching circuit is 10 ± 1 and at resonance offers a resistive load line of 1K ohms to the transistor.

Table 10 - Design Characteristics

for Frequency Mixer 2.1 Mc Output

Requirements 1/	Minimum	Design Center	Maximum
Input Frequency:			
Input #1		0.1 Mc	
Input #2		2.0 Mc	
Output Frequency		2.1 Mc	
Input Level			
Input #1		235 mV rms	
Input #2		100 mV rms	
Input Resistance:	1K		
Cross talk between inputs	23 db		
Output Amplitude			
at 1.8 Mc			4 mV. rms.
at 1.9 Mc			33 mV. rms.
at 2.0 Mc			92 mV. rms.
at 2.1 Mc			76 mV. rms.
at 2.2 Mc			5 mV. rms.
Power Supplies		+6 volts	
		-6 volts	
Current Consumption		1 ma	
Operating Temperature			
Upper Limit	100°C		
Lower Limit			-10°C

1/ For an external load of 100 ohms in parallel with 100 picofarads. Q of matching circuit is 10 ± 1 and at resonance offers a resistive load line of 1K ohms to the transistor.

Table 11 - Design Characteristics

for Frequency Mixer 18 Mc Output

Requirements 1/	Minimum	Design Center	Maximum
Input Frequency:			
Input #1		2.0 Mc	
Input #2		16.0 Mc	
Output Frequency		18.0 Mc	
Input Level			
Input #1		235 mV rms	
Input #2		150 mV rms	
Input Resistance:	1K		
Cross talk between inputs	27 db		
Output Amplitude			
at 14 Mc			20 mV. rms.
at 16 Mc			50 mV. rms.
at 18 Mc			115 mV. rms.
at 20 Mc			11 mV. rms.
at 22 Mc			2 mV. rms.
Power Supplies		+6 volts	
		-6 volts	
Current Consumption		1 ma	
Operating Temperature			
Upper Limit	100°C		
Lower Limit			-10°C

1/ For an external load of 100 ohms in parallel with 30 picofarads. Q of matching circuit is 10 ± 1 and at resonance offers a resistive load line of 1K ohms to the transistor.

Table 12 - Design Characteristics

for Frequency Mixer 20 Mc Output

Requirements 1/	Minimum	Design Center	Maximum
Input Frequency:			
Input #1		2.0 Mc	
Input #2		18.0 Mc	
Output Frequency		20.0 Mc	
Input Level			
Input #1		235 mV rms	
Input #2		150 mV rms	
Input Resistance:	1K		
Cross talk between inputs	27 db		
Output Amplitude			
at 16 Mc			20 mV. rms.
at 18 Mc			53 mV. rms
at 20 Mc			51 mV. rms.
at 22 Mc			23 mV. rms.
at 24 Mc			6 mV. rms.
Power Supplies		+6 volts	
		-6 volts	
Current Consumption		1 ma	
Operating Temperature			
Upper Limit	100°C		
Lower Limit			-10°C

1/ For an external load of 100 ohms in parallel with 20 picofarads. Q of matching circuit is 10 ± 1 and at resonance offers a resistive load line of 1K ohms to the transistor.

3.3.4.7 Application of Basic Circuits in the Limiter

A limiter circuit is often used as the input stage for a system, for instance, in frequency synthesizers. The requirements of such a circuit are that it must handle a wide range of input levels, should present a slight load to the source supplying the signal and supply a constant output signal to the system. This output voltage could be either a sinewave or square wave depending on the particular requirements.

A circuit in this nature can be put together using two universal amplifiers and one or two auxiliary microminiature blocks to house the limiter diodes and resistors and the tuned circuit when a sine wave output is needed. The maximum physical dimensions for a limiter circuit supplying a sinewave output are 0.5 x 0.5 x 0.4 inches.

Figure 20 shows the schematic of a limiter circuit with sinusoidal output. Table 13 shows the design characteristics.

Figure 21 shows the schematic for the circuit with square wave output. Table 14 shows design characteristics.

The limiter with a sinosoidal output was tested at different temperatures. Figure 22 shows the output voltage of the limiter circuit as a function of input voltage for temperatures ranging from -10°C to +100°C.

Table 13 - Design Characteristics for Limiter - Sinusoidal Output
1 Mc Input

Requirements	Minimum	Design Center	Maximum
Input Level:			
Upper limit	10 volts rms		
Lower limit			0.1 volts rms
Input Capacitance	0 pf		5 pf.
Input Resistance		430 ohms	
Output Amplitude	0.9 volts rms		1.05 volts rms.
Output Voltage variation (for ± 5 percent supply voltage change)			1%
Output Load:			
Capacitance			120 pf
Resistance			250 ohms
Operating Temperature			
Upper Limit	100°C		
Lower Limit			-10°C
Power Supplies		+6 volts	
		-6 volts	
Current Consumption		15 ma	

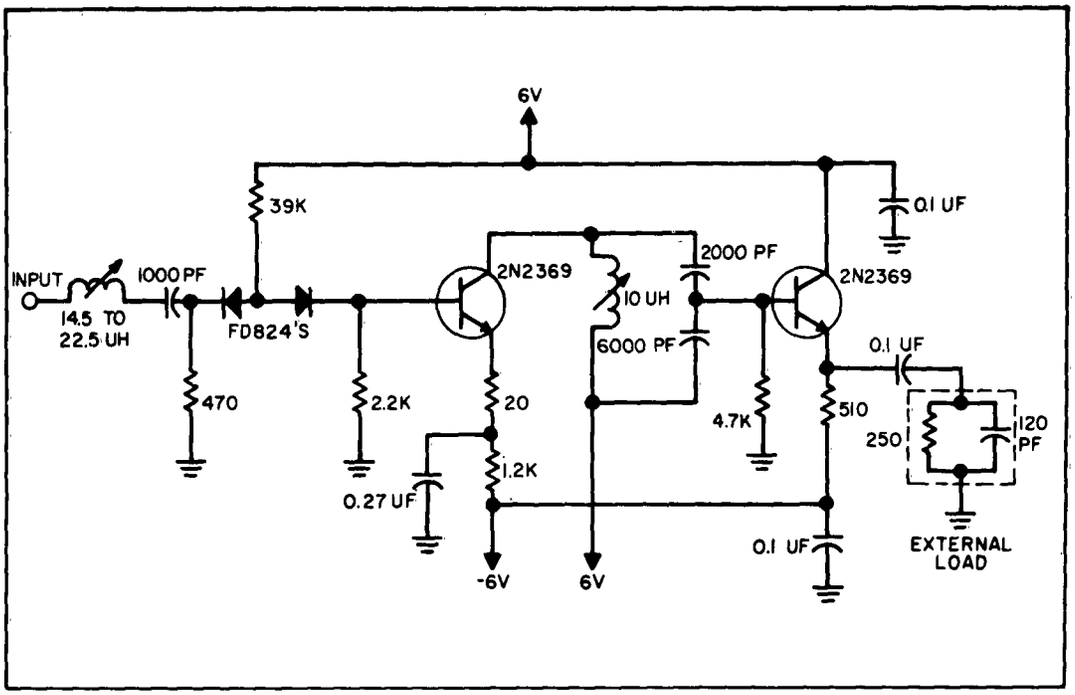


Figure 20. Limiter (Sinusoidal Output)

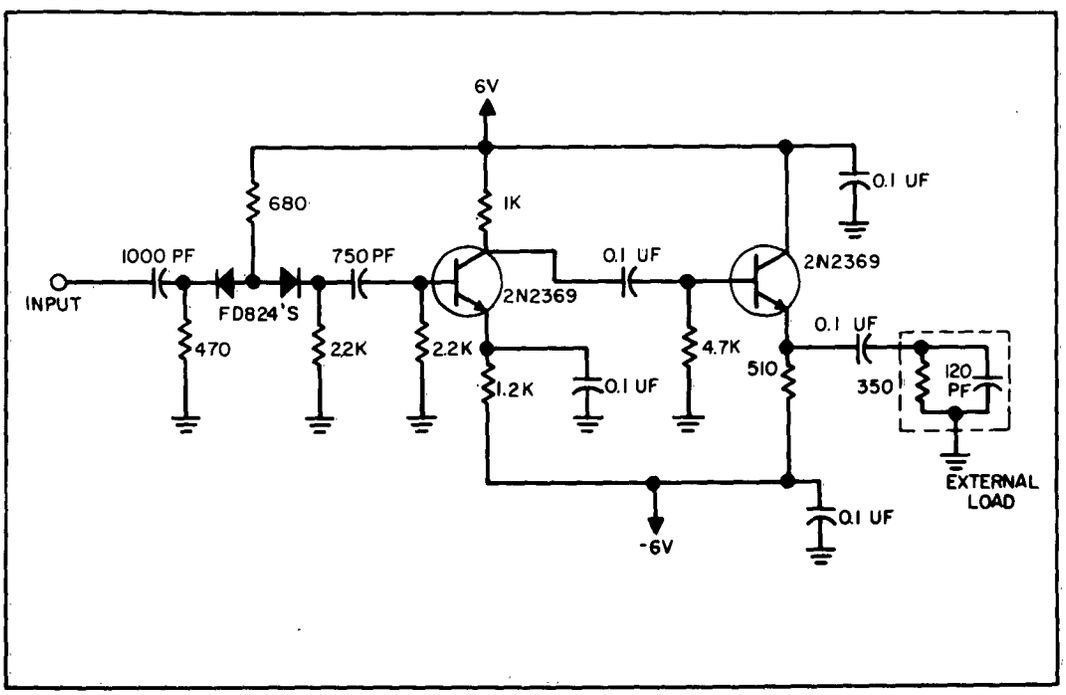


Figure 21. Limiter (Square Wave Output)

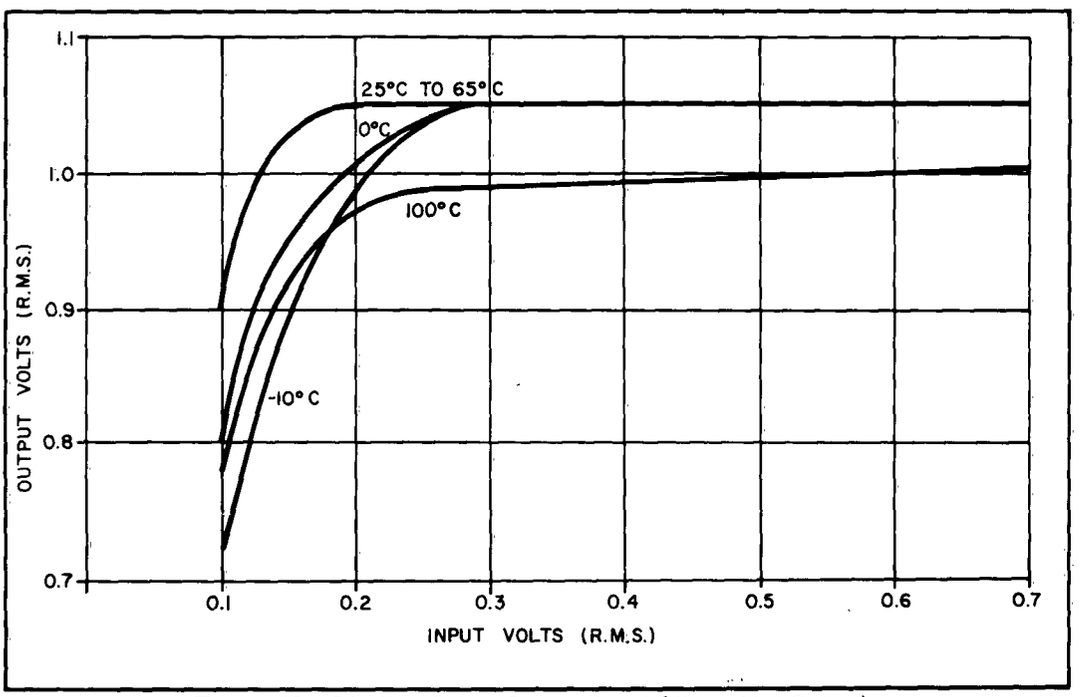


Figure 22. Limiter Output Versus Input (Sinusoidal Output)

Table 14 - Design Characteristics for Limiter - Square Wave Output

1 Mc Input

Requirements	Minimum	Design Center	Maximum
Input Level:			
Upper Limit	5 volts rms		
Lower Limit			0.2 volts rms.
Input Capacitance:		410 pf	
Input Resistance:		390 ohms	
Output Amplitude:	4.2 volts p.p.		5.4 volts p.p.
Output Voltage Variation (for ± 5 percent supply voltage change)			1%
Output Load:			
Capacitance			120 pf
Resistance			350 ohms
Operating temperature			
Upper Limit	100°C		
Lower Limit			-10°C
Power Supplies		+6 volts	
		-6 volts	
Current Consumption		15 ma	

3.3.4.8 Universal Microcircuit Block

The analog circuits shown in the preceding paragraphs performing the functions of r-f amplifiers, frequency multipliers, emitter followers and mixers, have common values of resistors and capacitors. This makes possible the design of a universal stage which can perform all the above functions by proper external connections. The following tabulation shows the values of these parts.

Function	R1	R2	R3	R4	R5	R6	R7	L1	C1	C2	C3	C4	C5	Q1
R.F. Amplifier	*	*	4.7k	20	560	560	*	See Text		"	*	1 mfd	0.2 mfd	2N2369
Freq. Multiplier	*	*	4.7k	20	560	560	*	"	"	"	*	1 mfd	0.2 mfd	2N2369
Mixer	1K	1K	4.7k	20	560	560	5.7K	"	"	"	*	1 mfd	0.2 mfd	2N2369
Emitter-Follower	*	*	4.7k	20	560	560	*	*	*	*	0.2 mfd	1 mfd	0.2 mfd	2N2369

*Part not required

Values of inductance L1 and capacitors C1 and C2 are dependent on operating frequency. (see next paragraph for further discussion).

Capacitors C4 and C5 are dependent on frequency band rather than on a particular operating frequency. Capacitor C4 is either used as a bypass of the -6 volts bus line or as emitter bypass, this eliminates the possibility of using it in common with other microcircuit blocks, and reduction in its capacitance value cannot be done. Capacitor C5 is the bypass for +6 volts supply in all cases. The correct value for frequencies below 300 kc is 1 microfarad, however, as it is used all the time as B+ bypass, its capacitance value can be decreased when several microcircuit blocks are connected to the same bus line. A value of 0.2 microfarads is thus adequate for C5.

Figure 23 shows the schematic of a universal circuit which contains all the non-frequency dependent components and can provide the four basic analog functions. With the exception of the capacitors, all components can be fabricated by thin film techniques on a substrate area of 0.1 square inches or less (0.3" x 0.3"). The number of required external leads, however, limits the number of circuits which can be accommodated on a given substrate. On a 15 lead, 1/2 inch square substrate, for example, there is enough area for at least three of the circuits (without capacitors) but only one can be used due to lead limitations.

The large capacitors required for C3, C4, and C5 cannot be fabricated at the present time, in thin film or integrated form. Tantalum capacitors, however, can be obtained in pellet form with the 1 microfarad value having a diameter of 220 mils by 40 mils thick.

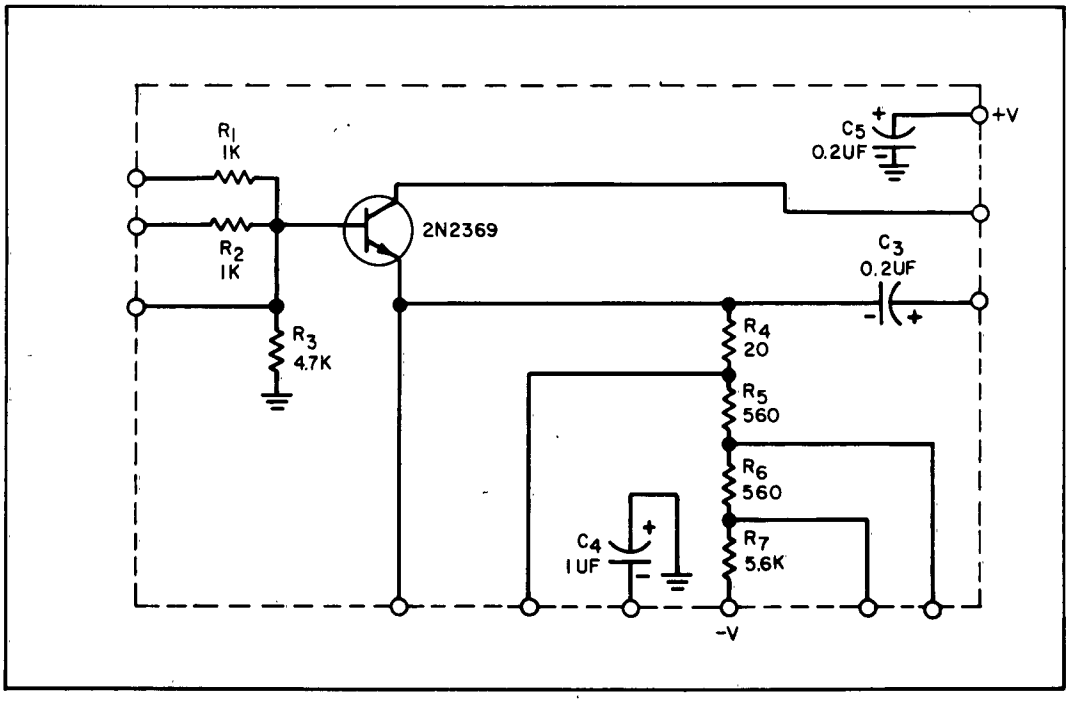


Figure 23. Universal Microcircuit Block

The 0.2 microfarad values measure 100 by 40 mils.* The additional area on a substrate, made available by lead limitations, can be used to mount and interconnect these pellet-type capacitors, thus making possible the fabrication of the entire circuit in a single block. Work completed on a Westinghouse sponsored development program has shown that this circuit can be fabricated in a 15 lead, 0.5 x 0.5 x 0.1" thin film encapsulated wafer by using the pellet capacitors for C3, C4, and C5. This wafer provides a common element for r.f. amplifiers, frequency multipliers, emitter-followers, and mixers over the required frequency range.

3.3.4.9 Auxiliary Tuned-Circuit Block

A tuned circuit is required in addition to the universal microcircuit block to perform the functions of r-f amplifying multiplying and mixing. Figure 24 shows the tuned circuit which is essentially a pi-network providing both selectivity and impedance matching.

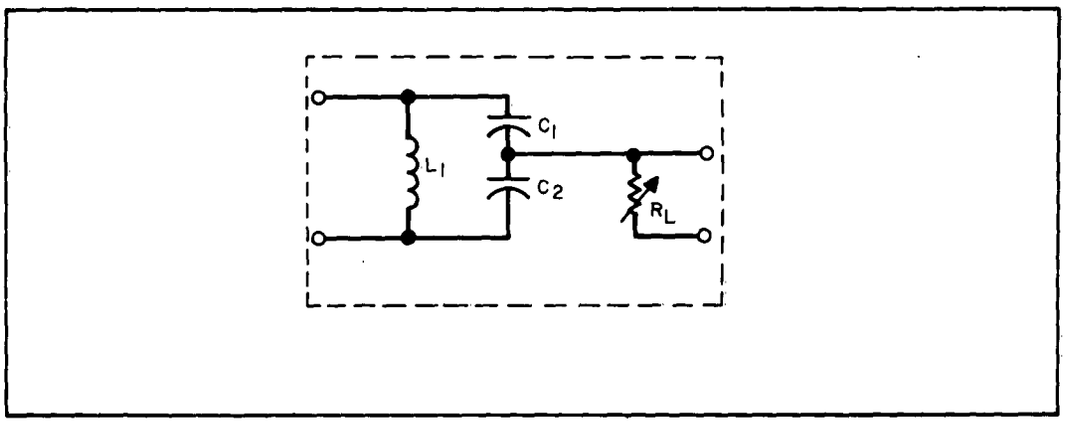


Figure 24. Auxiliary Tuned Circuit Block

Two basic problems have been considered and solved so that this circuit can be fabricated in micro-miniature form. The problem of tuning has been solved by designing with relatively low loaded Q's. This allows C_1 to be step-tunable and this type of capacitor can be fabricated in thin-film form. The dynamic impedance (L/C ratio) is also selected so that the selectivity is dependent principally on R_L and the coil Q rather than on the transistor amplifier input and output impedances. Thus, the tuned-circuit can be adjusted independent of the amplifier and it will not be detuned when connected to the universal microcircuit block. The lower loaded Q's also allow the coil L_1 to be of lower Q and thus more easily available in smaller sizes. The requirements on R_L also can be satisfied by step-adjustability which can be accomplished with thin-film resistor techniques.

* Capacitors of this type can be obtained from TRANSITOR ELECTRONICS, INC. Bennington, Vermont

Work completed on the Westinghouse sponsored development program has shown that the tuned circuit blocks can also be fabricated in a 0.5 x 0.5 x 0.1 inch wafer using components which are presently available. Larger sizes of C_1 and C_2 are obtained by using ceramic pellet capacitors[1] in parallel with the step-adjustable thin-film capacitors. Inductors used are of the toroidal type such as those available from VANGUARD.[2]

The following tabulation shows the values for L1, C1, and C2 for various frequencies.

Frequency	L1	C1	C2
0.1 Mc	110 μH	30000 pfd.	67000 pfd.
1 Mc	10 μH	2000 pfd.	6800 pfd.
10 Mc	1 μH	300 pfd.	680 pfd.
20 Mc	0.5 μH	150 pfd.	330 pfd.
30 Mc	0.35 μH	100 pfd.	220 pfd.

3.3.5 Analog Gate

The analog gate is designed to switch 2 to 3 mc sinewaves at rates up to 100 kc. In the "off" condition attenuation of at least 80 db is required. In the "on" condition, minimum attenuation is desired. Switching of the gate should not produce transients which would saturate the circuitry following the gate. Harmonic distortion should be kept to a minimum, although it is not critical, because any harmonically related frequencies will be subsequently filtered out.

The schematic of the analog gate is shown in figure 25. When a positive voltage is applied at the gating terminal, diode D_1 is forward biased and diodes D_2 and D_3 are reverse biased. Reverse biased diodes have a capacitance of 1 pf. This is equivalent to 53k ohms at 3 mc. Diode D_1 is forward biased and has an AC impedance of 30 ohms. Hence, the analog signal is greatly attenuated. This attenuation is a function of the output load. For the load encountered in the synthesizer a theoretical attenuation of 105 db is possible. The measured attenuation was 88 db which was near the measuring limit of the instruments used.

When a negative voltage is applied at the gating terminal, diode D_1 is back biased and diodes D_2 and D_3 are forward biased. Thus, an analog signal can now propagate from the input to the output with very low attenuation. Almost all of the attenuation of this circuit occurs at the 120 pf capacitor. The capacitor has been made small in order to allow fast switching of the gate. If the fast switching characteristic is not required, this capacitor can be made larger.

1. Such as those available from SCIONICS size 0.1 x 0.1 x 0.03"
2. Vanguard Electronics Co., Series 92 HF Subminiature Toroidal Inductors Q's 50 to 70, 0.2 x 0.2 x 0.1"

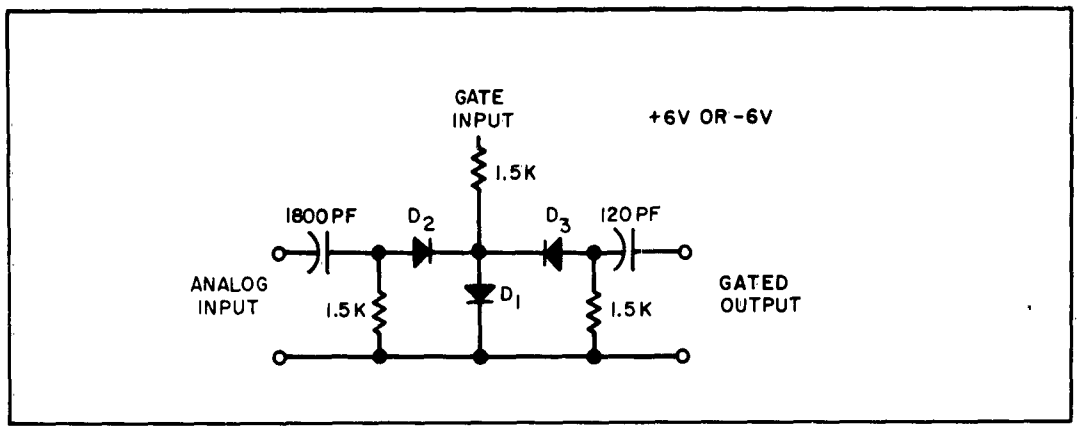


Figure 25. Analog Gate

Analog Gate Design Characteristics (see also figure 25)

Requirement	Minimum	Design Center	Maximum
Input Level of analog signal			.50 volts
load = 500			
Input Frequency		2 to 3 mc	
Input Impedance			
Gate enabled-unloaded	450		
-shorted	250		
Gate inhibited	1.4K		
Attenuation	80 db		
Gating Waveform			
Gate enabled		-6 V	
Gate Inhibited		+6 V	
Gating waveform rise and fall time			.6 μsec
Repetition rate of gating waveform	100 Kc	limited only by rise and fall times	
Temperature Range			
Upper	+65°C		
Lower			0°C

3.3.6 Squaring Circuit

The squaring circuit was developed to provide drive for the Decade Divider or any other circuit which required a square wave input. The squarer must operate over a frequency range of 100 KC - 30 MC, with a sine wave input, and be able to supply a waveform with fall times of less than 15 nsec. The falling edge is most important since it is this edge which triggers the flip-flop.

The required square wave could be generated with a number of cascaded switching stages; however, at low frequencies the number of stages required to obtain the desired 15 nsec fall time would be prohibitive. For this reason, it was felt that circuits employing regenerative feedback should be investigated. The circuits considered are discussed in the following paragraphs.

3. 3. 6. 1 Capacitive Feedback Squarer

The circuit in figure 26 was tested as a squarer with the Decade Divider as a load. Capacitive feedback between the output collector and the input base is provided in order to decrease the turn-off and turn-on times at low frequencies. Tests were conducted over a temperature range from 25°C to 60°C with input frequencies from 100 kc - 30 mc. Circuit operation was satisfactory below 10 mc, however, at higher frequencies the rise time deteriorated. This resulted in a decreased amplitude of the square wave output. This circuit also exhibited a tendency to oscillate at frequencies around 100 KC.

3. 3. 6. 2 Schmitt Trigger Squarer

Two similar Schmitt Trigger configurations were investigated. Figures 27 and 28 show the circuit diagrams for these configurations. The circuit in figure 27 was the first to be tested. The purpose of this test was to see if it was possible to use a Schmitt Trigger

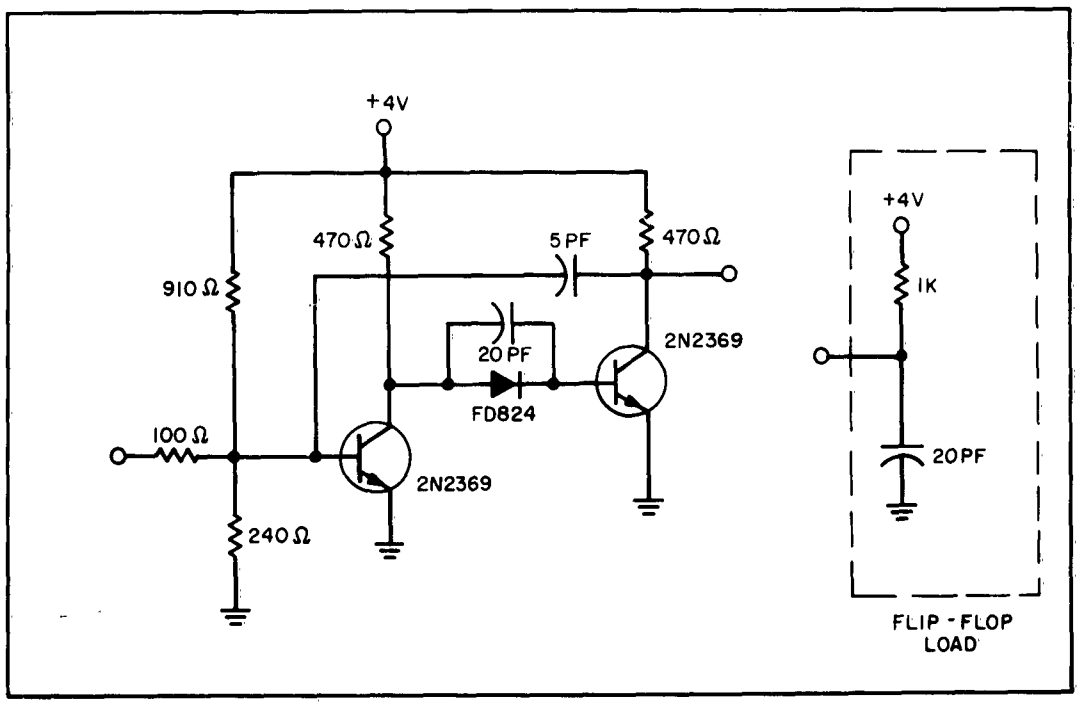


Figure 26. Capacitive Feedback Squarer

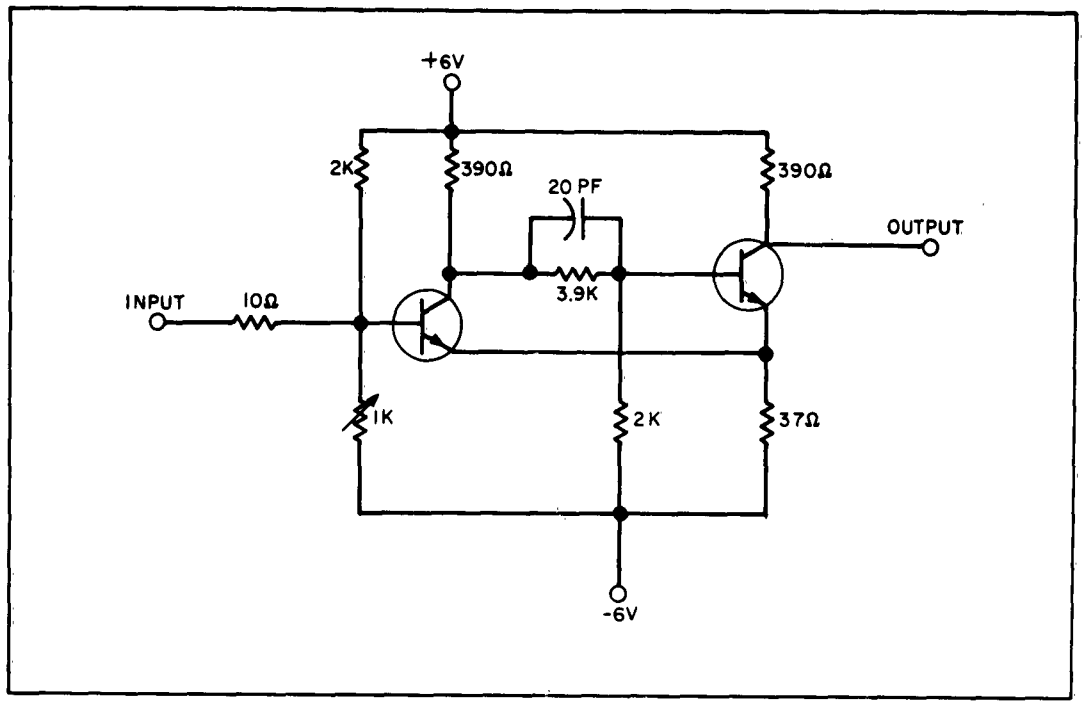


Figure 27. Schmitt Trigger (Basic)

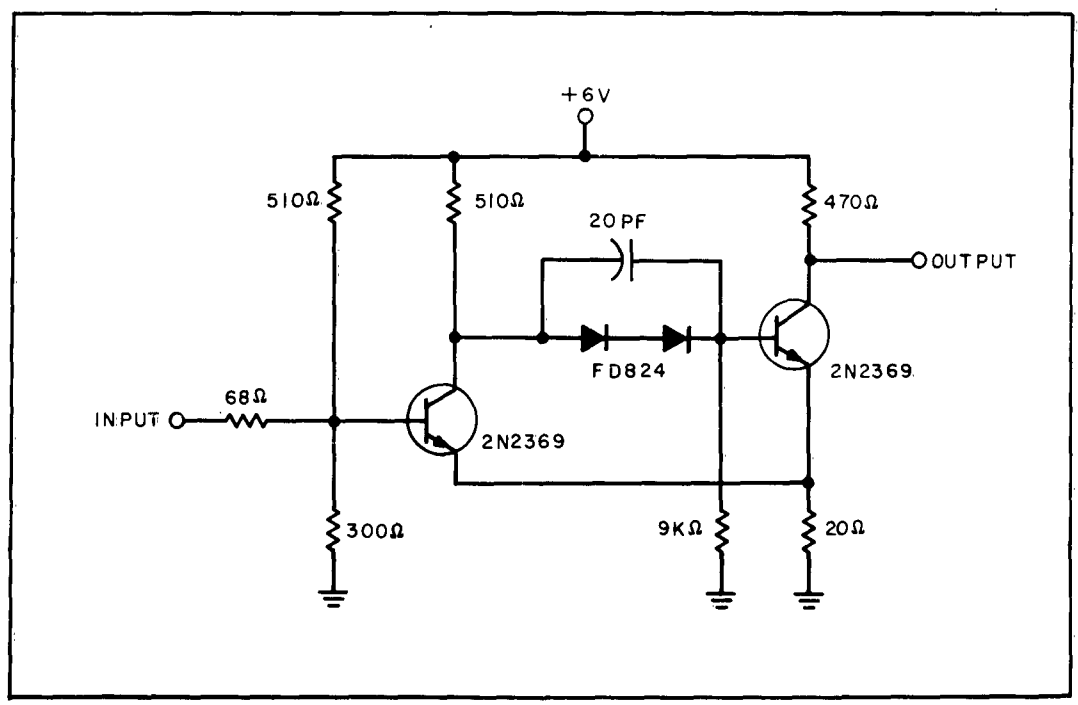


Figure 28. Schmitt Trigger Squarer

to supply the required square wave. A published circuit configuration was used to determine if the basic approach was feasible. A flip-flop load was simulated as shown in figure 27. These tests indicated that a Schmitt Trigger could be used to drive the flip-flop over a frequency range from 0.5-50 mc. Work was then started on the design of a Schmitt trigger which would consume less power than Configuration A, and which would be more suitable for this particular application. The circuit resulting from this work appears in figure 28. Tests were conducted using the Decade Divider as a load. The Schmitt trigger was found to operate properly over a temperature range from 0-100°C with input frequencies from 100 kc - 30 mc.

3. 3. 6. 3 Specifications

The test results obtained for the two types of squarers indicate that the Schmitt Trigger is the better for this application. Its operation is satisfactory over a wider frequency range than the capacitive feedback circuit. Moreover, it showed no tendency to give a spurious output at the lower frequencies. The specifications for the Schmitt Trigger as determined by the lab tests appear in Table 15.

Further tests were conducted to determine if the squarer could be driven directly from the limiter, as in figure 29. It was found that the squarer operated properly but the output of the emitter follower was distorted and could, therefore, not be used to drive any additional circuitry. This problem could be overcome with the addition of another common emitter stage. Two possible configurations are shown in figure 30.

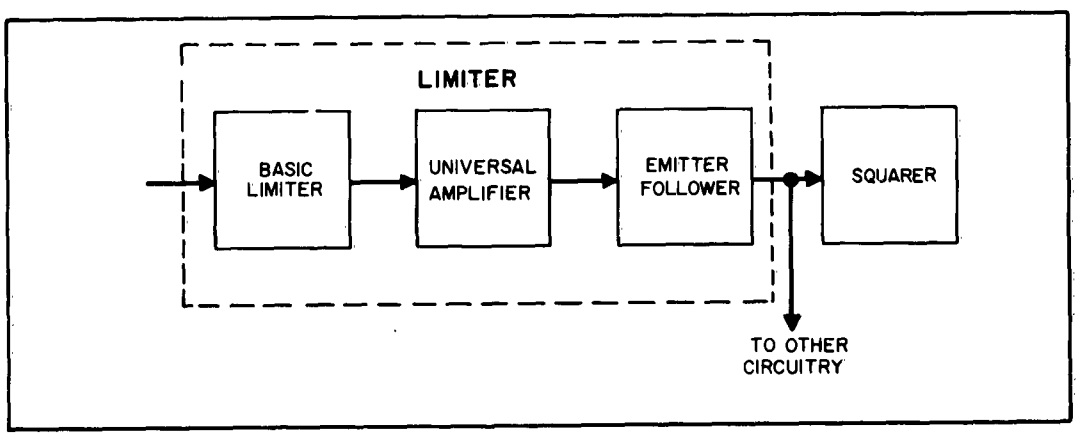


Figure 29. Limiter Overloading Problem

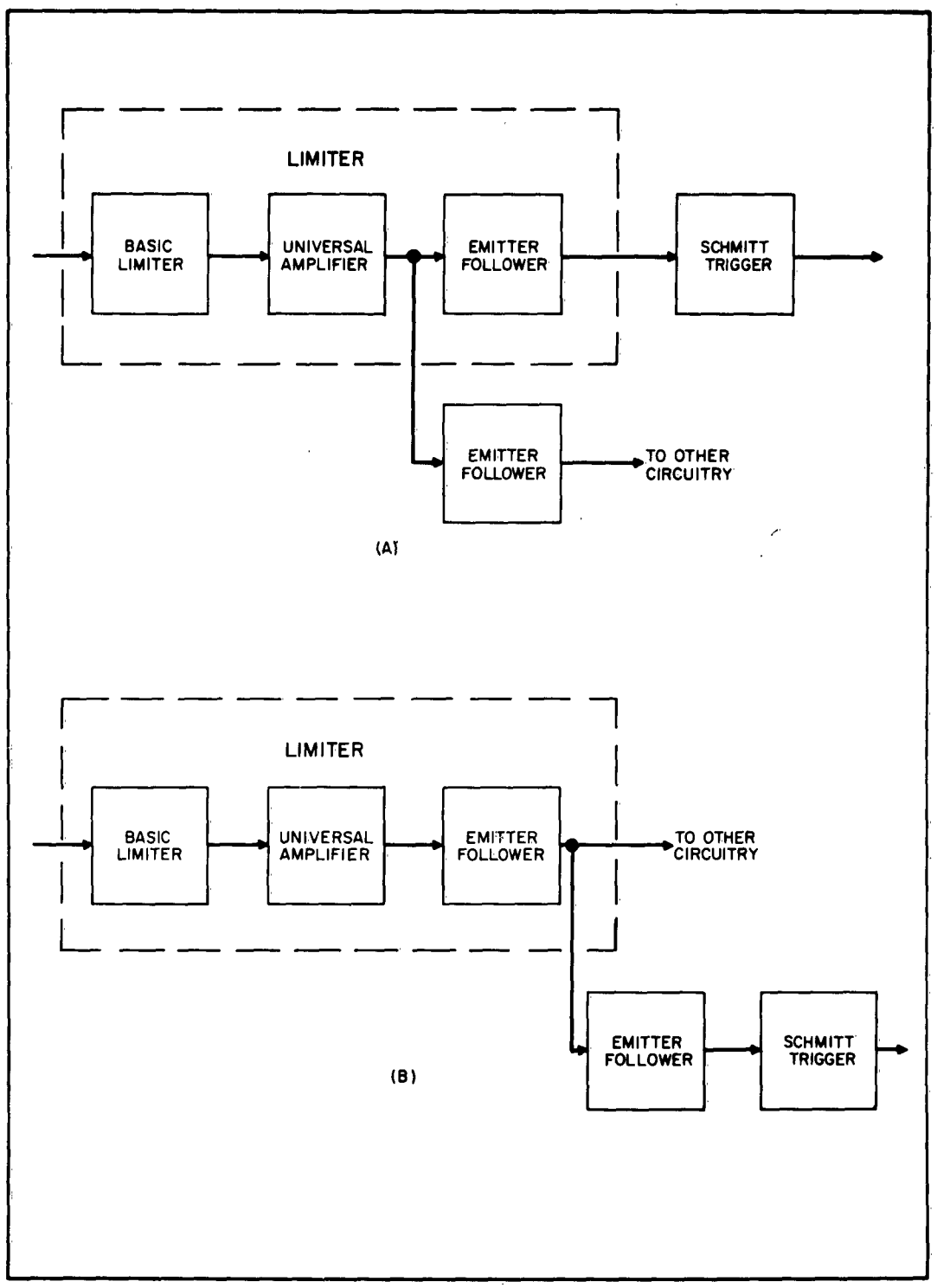


Figure 30. Driving Squarer from Limiter

TABLE 15

SPECIFICATION FOR SCHMITT TRIGGER (FIGURE 28)

	Minimum	Typical	Maximum
Input Impedance		112 Ω	
		62 pf	
Input Voltage		1V rms	
Operating Frequency	100 kc		30 mc
Operating Temperature	0°C		100°C
Supply Voltage		6V±5%	
Output Signal Amplitude		4V	
Output Rise Time		20 nsec	40 nsec
Output Fall Time		10 nsec	15 nsec
Loading	1K to +4V; 40 pf to gnd, (Flip-Flop + 20 pf)		

3.4 CRYSTAL FILTER STUDY

The problem of providing sharp rejection filters in a very small volume is a very difficult circuit design problem. Both RC and LC filters have been investigated. In addition, it was felt that an inquiry into crystal filters should be made.

In the past, crystal filters have generally been bulky and expensive. With the requirements imposed by transistorized circuitry, the size of these filters has been reduced somewhat. However, most of the filters available as off the shelf items are still too large for use in miniaturized circuits. One of the reasons for the large size of these filters is that there has been little demand for extremely small filters. Crystal cans are several times larger than the crystals inside. Special techniques for halving the number of crystals needed to perform a given function have been reported, but little work has been done to realize these designs.

To learn just what the state-of-the-art in crystal filter design is at the present time, a filter specification was written and distributed to 15 crystal filter manufacturers. To date - five replies have been received. A copy of the request is shown below followed by tables summarizing the replies:

MICROMINIATURE CRYSTAL FILTER SPECIFICATION

This specification describes a set of 13 types of crystal filters needed for use in a microminiature system. Crystal filters have been considered for use in this system because of their desirable electrical properties.

Where the specifications called for cannot be met the closest values to the ones specified should be used. If the specifications present undue design difficulties - two responses are required, one design would meet the original specification and the other design would meet a relaxed specification.

The information requested therefore is:

(1) Can the filters be designed as specified?

(2) If only some of the specifications can be met a filter with modified specifications should be presented. An indication of development costs and difficulties necessary to meet the original specifications should be presented where possible.

(3) Approximate price of filters in single and large quantities.

(4) Approximate delivery time.

ELECTRICAL SPECIFICATIONS

A. FILTER #1

1. Frequency - 2.0 mc - Only a single frequency will be passed. Hence, the pass band of the filter should be made only wide enough to pass this frequency under worst case conditions.

2. Shape Factor - Attenuation of 100 db at frequencies 100 KC away from the center frequency (on both sides of the center frequency).

3. Ultimate Attenuation - Attenuation of 100 db at all frequencies 100 KC or more from the center frequency. For both the Shape Factor and Ultimate Discrimination an estimate for an 80 db figure should be presented if it substantially differs from the 100 db figure.

4. Pass Band Ripple - Not applicable since only one frequency will be passed.

5. Impedance Level - The impedance levels of the input and output circuitry can be adjusted between 50 ohms and 10K. A figure around 1K is preferable. Also, please state maximum capacitive load that can be tolerated.

6. Insertion Level - Not important but should be kept to a minimum.

B. FILTERS #2 THROUGH #10

The specifications for these filters are the same as for filter #1 with the exception of the center frequency. In each case the filter is required to pass only a single frequency. The frequencies are as follows:

Filter No.	Center Frequency
#2	2.1 mc
#3	2.2 mc
#4	2.3 mc
#5	2.4 mc
#6	2.5 mc
#7	2.6 mc
#8	2.7 mc
#9	2.8 mc
#10	2.9 mc

C. FILTER #11

1. Frequency - 16 mc. single frequency
2. Shape Factor - Attenuation of 100 db at 14 and 18 mc.
3. Ultimate Attenuation - Attenuation of 100 db below 14 mc and above 18 mc.
4. through 6 - same as for filter #1

D. FILTER #12

1. Frequency - 18 mc - single frequencies
2. Shape Factor - Attenuation of 100 db at 16 and 20 mc.
3. Ultimate Attenuation - Attenuation of 100 db below 16 mc and above 20 mc.
4. through 6. same as for filter #1.

E. FILTER #13

1. Frequency - 18.0 mc to 18.1 mc - one db down max.
2. Shape Factor - 60 db/3 db, 2:1
3. Ultimate Attenuation - 100 db
4. Pass Band Ripple - 1 db
5. Impedance level - Same as for filter #1
6. Insertion loss - Same as for filter #1

MECHANICAL SPECIFICATIONS

A. Size - 0.5" x 0.5" x variable length. It is realized that this is a very difficult requirement to meet. Other geometrical configurations will be considered. In general a minimum voltage possible should be specified.

B. Reliability - MTBF data or any other reliability data should be presented.

C. Temperature Range - -55°C to +90°C

Summary of Manufacturers Replies for Filters 1 to 10

Manufacturer	Price		Size	Delivery	Impedance	Attenuation
A	1	$450	5/8"x7/8" x3-3/4"	10-12 wks.	400 Ω up to 150 pf	100 db
	10	$170				
	100	$ 95				
	1000	$ 63				
	1	$450	5/8"x7/8" x 2-3/4"	10-12 wks.	400 Ω up to 150 pf	80 db
	10	$140				
	100	$ 75				
	1000	$ 50				
B	Development $700		.5" x .5" x 1.85" More Desirable Size .65"x .75"x 2.0"	17-21 wks. production 12 wks. later	30 pf max.	100 db
	Production $30					
C	1	$171	.5"x.875" x 3	8-12 wks.		
	5	$144				
	10	$130				100 db
	25	$106		10-12 wks. for production		
	100	$ 76				
	500	$ 48				
	1000	$ 38				
			.5"x.625" x 2.0"			80 db
D	1	$2000	.5"x1.0" x 1.0"	16 wks.		80 db
	10	$300				60 db preferred
E	1	$300	1/2x7/8x 2-1/2	10-12 wks		100 db
	5	$150				
	10	$130				
	25	$110				
	100	$ 90				
	500	$ 75				
	1000	$ 60				

Summary of Manufacturers Replies for Filters 11 and 12

Manufacturer	Price		Size	Delivery	Impedance	Attenuation
A	1	$550	5/8"x3/4" x 3"	10-12 wks.	400Ω to 150 pf with impedance transformation	100 db
	10	$185				
	100	$103				
	1000	$ 68				
	1	$550	5/8"x3/4" x 2-1/2"	10-12 wks.	same as for 100 db	80 db
	10	$155				
	100	$ 85				
	1000	$ 57				

Summary of Manufacturers Replies for Filters 11 and 12 (Continued)

Manufacturer	Price	Size	Delivery	Impedance	Attenuation
B	development over $700 Production $30	.5"x.5" x 1.85"	17-21 wks. production 12 weeks later	5 pf	100 db
C	1 $128 5 $118 10 $109 25 $ 87 100 $ 61 500 $ 39 1000 $ 32	.5"x.5" x 2.0"	8 to 12 wks. 10-12 wks. production		
D	1 $1500	.5"x.75" x 1.0"	16 wks.		80 db 60 db preferred
E	1 $300 5 $150 10 $130 25 $110 100 $ 90 500 $ 75 1000 $ 60	1/2"x 13/16"x 2-3/8"	10-12 wks.		

Summary of Manufacturers Replies for Filter 13

Manufacturer	Price	Size	Delivery	Impedance	Attenuation
A	1 $650 10 $380 100 $190 1000 $116	3/4"x 1-7/16" x3-1/32"	10-12 wks.	400 Ω and up to 150 pf	up to 70 db
B	prototype $1500 Production $80	.5"x.5" x 3.0" with 2 db ripple	17-21 wks.		2 db, bandwidth less than 55 KC -ripple 2 db
C	1 $205 5 $171 10 $153 25 $125 100 $ 90 500 $ 59 1000 $ 45	.625"x .75" x 2.0"	8-10 wks.		

Summary of Manufacturers Replies for Filter 13 (Continued)

Manufacturer	Price		Size	Delivery	Impedance	Attenuation
D	1	$1500	.5" x .75" x 1.0"			
E	1	$800	1/2" x 15/16" x 4-7/8"	12-14 wks.		
	5	$475				
	10	$375				
	25	$300				
	100	$200				
	500	$175				
	1000	$130				

From the table it can be seen that the size requirement is the hardest one to meet. From other correspondence it was learned that size could be reduced in the future, when crystal manufacturers reduce the size of the cans which house the crystals. Even now the dimensions of these filters are such that they can be used with miniaturized circuitry. For the present application, a width of .625" can be tolerated. Virtually all the manufacturers specified filters which will conform to this dimension.

Filters with bandwidths much less then 1% can be made easily. Larger bandwidths than 1% can be made but only at a penalty of larger size and poorer electrical characteristics. For single tone filters, 100 db attenuation outside of the passband can be obtained with 8 crystals. Six crystals can produce 80 db attenuation and four crystals can give 60 db attenuation. For these rejection levels, shielding is just as important as the number of crystals used. The shields are responsible for some of the bulk of the units.

A calculation was made to compare the performance of a tuned amplifier chain with that of a crystal filter. The relation used was

$$\left|\frac{K}{K_{res}}\right|^n = \frac{1}{\left[1 + (2\delta Q)^2\right]^{n/2}}$$

$$\delta = \frac{\omega - \omega_o}{\omega_o}$$

Q_e = effective Q of each stage

n = number of stages

K_{res} = impedance at resonance

K = impedance off resonance

ω_o = resonance frequency

ω = frequency off resonance

The calculations were made for f_o = 2.9 mc. $\frac{K}{K_{res}}$ was calculated at 3.0 mc and expressed in db

n	Q_e	K/K_{res} in db
5	10	-8
5	20	-23
5	30	-36
5	40	-46
5	50	-57

n	Q_e	K/K_{res} in db
10	10	-17
10	20	-46
10	30	-72
10	40	-92
10	50	-114

To get attenuation even close to 100 db, many high Q stages are needed. Although these stages could conceivably be packaged into a small volume, the problem of aligning them would not be easy. Furthermore, it is questionable whether one gains by replacing one filter with 10 active circuits.

A general conclusion reached from this study is that crystal filters can provide some very definite advantages over other filtering methods. Electrical characteristics of crystal filters are superior to other devices. The size of these units, on the other hand, presents a bit of a problem at the present time. However, a number of manufacturers are investigating methods for reducing volume by a factor of two or more.

3.5 SPECIAL PURPOSE CIRCUITS

The following special purpose circuits now exist as tentative designs:

(1) Monostable multivibrator
(2) Deflection plate amplifier
(3) Pulse amplifier
(4) DC amplifier
(5) Trigger unit (high gain squarer)

Item (1) is a new circuit. Items (2), (3), (4) appear to be modifications to the universal amplifier. Item (5) is a modification of the squarer.

4. CONCLUSIONS

Work in the past quarter has accomplished the following:

1. A listing of the load requirements for each circuit has been assembled.
2. The various microelectronic fabrication techniques of packaging have been evaluated. A flat package of the order of 1/2" x 1/2" x 1/10" is recommended to package each circuit. The packages should be interconnected on three sides by printed circuit boards and assembled into a module. The Amp Meca interconnection method is recommended.
3. Designs have been completed, temperature tests have been made, and specifications have been written for the following circuits:
   - Decade Divider (includes flip-flop and gate)
   - Digital Gate
   - Universal Amplifier
     - Grounded emitter amplifier
     - Frequency multiplier
     - Emitter follower
     - Frequency mixer
     - Limiter
   - Analog Gate
   - Squaring Circuit
4. The microminiature crystal filter evaluation is substantially complete. Current results show crystal filter performance to be superior to other approaches though filter size is larger than is desired. Development programs currently in process if successful are expected to reduce filter size by 2 times or more.
5. Special purpose circuit designs are under evaluation.

5. PROGRAM FOR THE NEXT INTERVAL

The following work is scheduled for the next period:

1. The microminiature crystal filter evaluation will be completed.
2. Special purpose circuit breadboards will be completed.
3. Specifications for the special purpose circuits will be written.
4. Circuit layouts will be completed.
5. Component evaluation will be completed.

APPENDIX A

CIRCUIT LOADING REQUIREMENTS

1. Flip-Flop Requirements

SYSTEM	DRIVEN BY	DRIVES
Frequency Counter	*Squarer at 1 mc	1 - Decade Divider and 1 - Squarer
	*Decade Divider 100 kc	1 - Decade Divider
	*Decade Divider 10 kc	1 - Decade Divider and 1 - Squarer
	*Decade Divider 1 kc	1 - Decade Divider and 1 - Squarer
	*Decade Divider 100 cps	1 - Decade Divider and 1 - Squarer
	*Decade Divider 10 cps	1 - Decade Divider and 1 - Squarer
	*Squarer 0-10 mc	1 - Blanking and Reset Unit
	*Gate 0-10 mc	1 - Decade Divider and Readout Logic
	*Decade Divider 0-1 mc	1 - Decade Divider and Readout Logic
	*Decade Divider 0-100 kc	1 - Decade Divider and Readout Logic
	*Decade Divider 0-10 kc	1 - Decade Divider and Readout Logic
Frequency Counter	*Decade Divider 0-1 kc	1 - Decade Divider and Readout Logic
	*Decade Divider 0-100 cps	1 - Decade Divider and Readout Logic
	*Decade Divider 0-10 cps	1 - Decade Divider and Readout Logic
	*Decade Divider 0-1 cps	Readout Logic
	Decade Divider or Squarer 0 to 1 mc	1 - Digital Gate
Time Comparator	*Squarer 1 mc	1 - Decade Divider
	*Decade Divider 100 kc	1 - Decade Divider and 1 - Emitter Follower
	Decade Divider 10 kc (in Quinary Divider)	1 - Flip-Flop
	Quinary Divider 2 kc	1 - Resolver (500 Ω tuned to 1 kc)

* In this application the flip-flop is part of a Decade Divider.

SYSTEM	DRIVEN BY	DRIVES
	*Squarer 1 kc	1 - Decade Divider and 1 - Emitter Follower
	*Decade Divider 100 cps	1 - Decade Divider and 1 - Emitter Follower
	*Decade Divider 10 cps	1 - Pulse Amplifier 1 - Emitter Follower
Frequency Deviation Meter	*Squarer 1, 2.5, 5 mc	1 - Quinary Divider and 1 - Flip-Flop
	*Quinary Divider 0.5, 1 mc	1 - Flip-Flop and 1 - Amplifier
	Quinary Divider 200 kc	1 - Amplifier
Frequency Standard	*Squarer 5 mc	1 - Decade Divider and 1 - Amplifier
	Quinary Divider, 1 mc (part of Decade Divider)	1 - Amplifier
Frequency Synthesizer	Squarer, 1 mc (part of Decade Divider)	1 - Amplifier
	Mixer 20 mc (part of Decade Divider)	1 - Mixer

2. Digital Gate Requirements

SYSTEM	DRIVEN BY	DRIVES
Frequency Counter	2 - Flip-Flops 1 mc	Flip-Flop
	2 - Flip-Flops 1 mc	Flip-Flop
	2 - Flip-Flops 100 kc	Flip-Flop
	2 - Flip-Flops 100 kc	Flip-Flop
	2 - Flip-Flops 10 kc	Flip-Flop
	2 - Flip-Flops 10 kc	Flip-Flop
	2 - Flip-Flops 1 kc	Flip-Flop
	2 - Flip-Flops 1 kc	Flip-Flop
	2 - Flip-Flops 100 cps	Flip-Flop
	2 - Flip-Flops 100 cps	Flip-Flop
	2 - Flip-Flops 10 cps	Flip-Flop
	2 - Flip-Flops 10 cps	Flip-Flop
	Schmitt Trigger and Reset and Blanking Unit	Counter

*In this application the flip-flop is part of a Quinary Divider.

SYSTEM	DRIVEN BY	DRIVES
Time Comparator	2 - Flip-Flops 1 mc	Flip-Flop
	2 - Flip-Flops 1 mc	Flip-Flop
	2 - Flip-Flops 100 kc	Flip-Flop
	2 - Flip-Flops 100 kc	Flip-Flop
	2 - Flip-Flops 10 kc	Flip-Flop
	2 - Flip-Flops 10 kc	Flip-Flop
	2 - Flip-Flops 1 kc	Flip-Flop
	2 - Flip-Flops 1 kc	Flip-Flop
	2 - Flip-Flops 100 cps	Flip-Flop
	2 - Flip-Flops 100 cps	Flip-Flop
	2 - Flip-Flops 10 cps	Flip-Flops
	2 - Flip-Flops 10 cps	Flip-Flops
Frequency Deviation Meter	2 - Flip-Flops 5 mc	Flip-Flops
	2 - Flip-Flops 5 mc	Flip-Flop
	2 - Flip-Flops 1 mc	Flip-Flop
	2 - Flip-Flops 1 mc	Flip-Flop
Frequency Standard	2 - Flip-Flops 5 mc	Flip-Flop
	2 - Flip-Flops 5 mc	Flip-Flop
	2 - Flip-Flops 1 mc	Flip-Flop
	2 - Flip-Flops 1 mc	Flip-Flop
Frequency Synthesizer	2 - Flip-Flops 1 mc	Flip-Flop
	2 - Flip-Flops 1 mc	Flip-Flop
	2 - Flip-Flops 20-21 mc	Flip-Flop

3. Frequency Multiplier Requirements

SYSTEM	DRIVEN BY	DRIVES
Frequency Counter	Squaring Circuit at 1 mc	Digital gate
Frequency Deviation Meter	(x10) Amplifier at 100 kc $+\Delta f$	Mixer at 1000 kc $+10\,\Delta f$
	(x10) Mixer at 100 kc $+\Delta f$	Mixer at 1 mc $+ 100\Delta f$

SYSTEM	DRIVEN BY	DRIVES
	(x10) Mixer at 100 kc +100 Δf	Mixer at 1 mc + 1000Δf
	(x10) Mixer at 100 kc +1000 Δf	Mixer at 1 mc +10, 000 Δf
	(x3) Amplifier 100 kc ref	Mixer and x3 Multiplier
	(x3) Multiplier at 300 kc	Amplifier
	Amplifier at 900 kc	2 mixers
Frequency Synthesizer	Squarer 1 mc input	x4 Multiplier and x5 Multiplier
	(x4) Multiplier 4 mc input	4 - Mixers
	(x5) Multiplier 4 mc input	Mixer

4. Frequency Mixer Requirements

SYSTEM	DRIVEN BY	DRIVES
Frequency Deviation Meter	Limiter at 1 mc +Δf and Amplifier at 900 kc	Analog Gate at 100 kc + Δf
	Limiter at 2. 5 mc + Δf and Mixer at 2400 kc	Analog Gate at 100 kc + Δf
	Limiter at 5 mc + Δf and Mixer at 5100 kc	Analog Gate at 100 kc + Δf
	x10 Multiplier at 1 mc +10 Δf and amplifier at 900 kc	x 10 Multiplier and Analog Gate } at 100 kc + 10 Δf
	x 10 Multiplier at 1 mc +100 Δf and amplifier at 900 kc	x 10 Multiplier and Analog Gate } at 100 kc + 100 Δf
	x 10 Multiplier at 1 mc + 1000 Δf and amplifier at 900 kc	x 10 Multiplier and Analog Gate at 100 mc +1000 Δf
	x 10 Multiplier at 1 mc +10, 000 Δf and amplifier at 900 kc	Analog Gate at 100 kc 10, 000 kc
	Analog Gate at 100 kc + Δf to 10, 000 Δf and Amplifier at 100 kc	Filter followed by dc amplifier
	x3 Multiplier at 2700 kc and x3 Multiplier at 300 kc	Two mixers at 2400 kc (+Ref.)
	x3 Multiplier at 2700 kc and x3 Multiplier at 2400 kc	Mixer at 5100 kc

SYSTEM	DRIVEN BY	DRIVES
Frequency Synthesizer	x5 Multiplier at 20 mc and Mixer thru Filter at 20-21 mc	Amplifier at 0-1 mc
	x4 Multiplier at 16 mc and Frequency Divider at 2.0x mc thru filter	Mixer thru Filter at 18.ox mc
	Pulse Network thru Filter at 2 mc and x4 Multiplier at 16 mc thru filter	Mixer thru Filter at 19 mc
	x4 Multiplier at 16 mc and Frequency Divider at 2.0 xx mc thru filter	Mixer thru Filter at 18.0xx mc
	x4 Multiplier at 16 mc and Frequency Divider at 2.0 xxx mc thru filter	Mixer thru Filter at 18.0xxx mc
	Mixer thru Filter at 18 mc and Pulse Network thru Filter at 2.x mc	Squarer thru Filter at 20.x mc
	Mixer thru Filter at 18.0x mc and Pulse Network thru Filter at 2.x mc	Squarer thru Filter at 20.xx mc
	Mixer thru Filter at 18.0xx mc and Pulse Network thru Filter at 2.x mc	Squarer thru Filter at 20.xxx mc
	Mixer thru Filter at 18.0xx mc and Pulse Network thru Filter at 20.xxxx mc	Mixer thru Filter at 20.xxxx mc

5. Amplifier Requirements

SYSTEM	DRIVEN BY	DRIVES
Frequency Counter	Frequency Dividers at 1, 10, 100, 1000, 10,000, 100,000 cps	Schmitt Trigger
Time Comparator	Decade Divider at 1 cps	1 pps output
	Decade Divider at 10 kc	10 kc output
	Squarer at 1 kc	1 kc output
	Decade Divider at 100 cps	100 cps output
	Decade Divider at 10 cps	10 cps output
	Decade Divider at 1 cps	1 cps output

SYSTEM	DRIVEN BY	DRIVES
Frequency Deviation Meter	Analog Gate 100 kc + Δf to 100 kc + 10,000 Δf	Horizontal input of scope
	Amplifier 100 kc Ref.	Vertical input of scope
	Mixer thru Low Pass Filter Δf to 10,000 Δf	Recorder/Indicator
	Analog Gate 100 kc	x3 Multiplier, Voltage Amplifier, Mixer
	x3 Multiplier at 900 kc	3x Multiplier, Five Mixers
Frequency Standard	Oscillator at 5 mc	5 mc output
	5:1 Divider at 1 mc	1 mc output
	Decade Divider at 100 kc	100 kc output

6. Analog Gate Requirements

SYSTEM	DRIVEN BY	DRIVES
Frequency Deviation Meter	(1) 00 kc + Δf to 5 mc + Δf from Squarer or	Amplifier at 100 kc + Δf
	(2), (3), (4) 100 kc + Δf from one of three mixers	
	(1) 100 kc + Δf from Amplifier (2) " + 10 Δf from Mixer (3) " + 100 Δf from Mixer (4) " + 1000 Δf from Mixer (5) " + 10,000 Δf from Mixer	Amplifier and Mixer
	(1) Binary Divider 2 kc-100 kc (2) Quinary Divider 4 kc-200 kc (3) Binary Divider 10 kc-500 kc (4) Squarer 100 kc to 5 mc	Amplifier
Frequency Synthesizer	Amplifier at 20 mc	Mixer

7. Squarer Requirements

SYSTEM	DRIVEN BY	DRIVES
Frequency Counter	Standard Frequency (Internal or External) 1 mc	1 - Times 10 Mult. and 1 - Decade Divider
	Trigger Unit or Decade Divider 1 cps to 1 mc	1 - Flip-Flop or 1 - Decade Divider and 1 - Blanking and Reset Unit
Time Comparator	Limiter 1 mc	1 - Decade Divider
	Resolver 1 kc	1 - Decade Divider and 1 - Emitter Follower

SYSTEM	DRIVEN BY	DRIVES
Frequency Deviation Meter	Limiter 0. 1, 1, 2. 5, 5 mc	1 - Quinary Divider and 1 - Amplifier
Frequency Standard	Oscillator, 5 mc	1 - Quinary Divider
Frequency Synthesizer	Limiter	1 - Decade Divider and 1 - Times 4 Multiplier

8. Trigger Unit Requirements

SYSTEM	DRIVEN BY	DRIVES
Frequency Counter	Frequency Input 0-10 mc	Squarer

9. Limiter Requirements

SYSTEM	DRIVEN BY	DRIVES
Frequency Counter	External Frequency Standard 1 mc	Squarer
Time Comparator	1 mc input	Squarer
Frequency Deviation Meter	Unknown Frequency Input (. 1, 1, 2	Analog Gate and Three Mixers
	Reference Frequency (. 1, 1, 2. 5, 5 mc)	Squarer
Frequency Synthesizer	1 mc Input	Squarer

10. Pulse Forming Networks

SYSTEM	DRIVEN BY	DRIVES
Frequency Synthesizer	Frequency Divider 100 kc	10 Filters

APPENDIX B

Part 1. AN IMPROVED METHOD OF DESIGNING Pi NETWORK

It is possible to calculate X_L, X_{C1}, and X_{C2} by accounting for the Q of the coil.

The formula for calculating X_L if the inductor has an infinite Q is given by:*

$$X_L = \left| \left(R_{in} R_L \sin\beta \right) \Big/ \left(R_L \cos\beta - \sqrt{R_{in} R_L} \right) \right|$$

For small positive angles β, X_L may be rewritten as

$$X_L = R_{in} R_L \sin\beta \Big/ \left(\sqrt{R_{in} R_L} - R_L \cos\beta \right)$$

In this equation R_{in} is the equivalent resistance presented by the ideal Pi network when loaded with R_L. The transistor sees a resistance R'_{in} which is the parallel combination of R_{IN} and the resistance R_c due to the finite Q of the coil. R'_{in} is given by

$$R'_{in} = R_{in} R_c / (R_{in} + R_c)$$

If this equation is solved for R_{in} in terms of R'_{in} the result is

$$R_{in} = R'_{in} R_c / (R_c - R'_{in})$$

By using this in the equation for X_L, it will be possible to determine X_L for the desired resistance R'_{in} if the unloaded Q of the coil is known

$$X_L = \frac{\left[R'_{in} R_c / (R_c - R'_{in}) \right] R_L \sin\beta}{\sqrt{\left(\frac{R'_{in} R_c}{R_c - R'_{in}} \right) R_L} - R_L \cos\beta}$$

But $R_c = Q_u X_L$, where Q_u is the unloaded Q of the coil.

$$X_L = \left[R'_{in} Q_u X_L / (Q_u X_L - R'_{in}) \right] R_L \sin\beta \Big/ \sqrt{\left(\frac{R'_{in} Q_u X_L}{Q_u X_L - R'_{in}} \right) R_L} - R_L \cos\beta$$

*"Radio Engineers Handbook", Frederick E. Terman, McGraw-Hill Book Co. 1943

Simplifying the above equation and collecting like terms yields:

$$a X_L^2 + b X_L + c = 0 \text{ where}$$

$$a = R'_{in} R_L - R_L^2 \cos^2\beta,$$

$$b = \frac{(R'_{in})^2 R_L}{Q_u} - 2 R_L^2 R'_{in} \cos\beta \left(\sin\beta - \frac{\cos\beta}{Q_u}\right) \text{ and}$$

$$c = \frac{2R'_{in} R_L^2}{Q_u} \sin\beta \cos\beta (R'_{in} - 1) - (R'_{in})^2 R_L^2 \left(\sin^2\beta + \frac{\cos^2\beta}{Q_u}\right).$$

Then

$$X_L = \left(-b \pm \sqrt{b^2 - 4ac}\right) / 2a$$

Once X_L has been determined, calculate R_c from $R_c = Q_u X_L$. Then find R_{in} from

$$R_{in} = R'_{in} R_c / (R_c - R'_{in}).$$

Then obtain X_{C1} and X_{C2} from* $X_{C1} = \sqrt{R_{in} R_L} \sin\beta$ and

$$X_{C2} = \left| R_{in} R_L \sin\beta \Big/ (R_{in} \cos\beta - \sqrt{R_{in} R_L}) \right|$$

Part 2. DETERMINATION OF RESISTANCE LOOKING BACK FROM LOAD

Referring to figure 12(b) the impedance looking left of C_2 is given by:

$$Z1 = \frac{R_3 J\omega L}{R_3 + J\omega L} + \frac{1}{J\omega C_1}$$

$$Z1 = \frac{-\omega^2 R_3 LC_1 + R_3 + J\omega L}{-\omega^2 LC_1 + J\omega R_3 C_1}$$

$$Y_1 = 1/Z1 = \frac{R_3 \omega^4 L^2 C_1^2 + J\omega^3 L^2 C_1 + J\omega R_3^2 C_1 (1-\omega^2 LC_1)}{R_3^2 (1-\omega^2 L C_1)^2 + \omega^2 L^2}$$

*"Radio Engineers Handbook", Frederick E. Terman, McGraw-Hill Book Co. 1943

The reactive portion of Y_1 will resonate with the capacitor C_2. The only portion seen looking back will then be the real part of Y_1. This real part when coverted to a resistance R_{seen} is given by:

$$R_{seen} = \frac{R_3^2 (1-\omega^2 L C_1)^2 + \omega^2 L^2}{R_3 \omega^4 L^2 C_1^2} = \frac{R_3^2 \left(1-\frac{X_L}{X_4}\right)^2 + X_L^2}{R_3 \left(\frac{X_L}{X_{C_1}}\right)^2} .$$

To verify that R_{seen} is equal to R_L if $R_3 = R_{in}$, the formulas for X_L and X_{C1} are substituted in the equation for R_{seen}

$$R_{seen} = R_{in}^2 \frac{\left[1 - \sqrt{R_{in} R_L}/\left(\sqrt{R_{in} R_L} - R_L \cos\beta\right)\right]^2}{R_{in}^2 R_L / \left(\sqrt{R_{in} R_L} - R_L \cos\beta\right)^2} +$$

$$\frac{\frac{R_{in}^2 R_L^2 \sin^2\beta}{\left(\sqrt{R_{in} R_L} - R_L \cos\beta\right)^2}}{R_{in}^2 RL/\sqrt{R_{in} R_L} - R_L \cos\beta^2}$$

$$R_{seen} = \frac{\left(\sqrt{R_{in} R_L} - R_L \cos\beta - \sqrt{R_{in} R_L}\right)^2 + R_L^2 \sin^2\beta}{R_L}$$

$$R_{seen} = \frac{(-R_L \cos\beta)^2 + R_L^2 \sin^2\beta}{R_L} = R_L$$